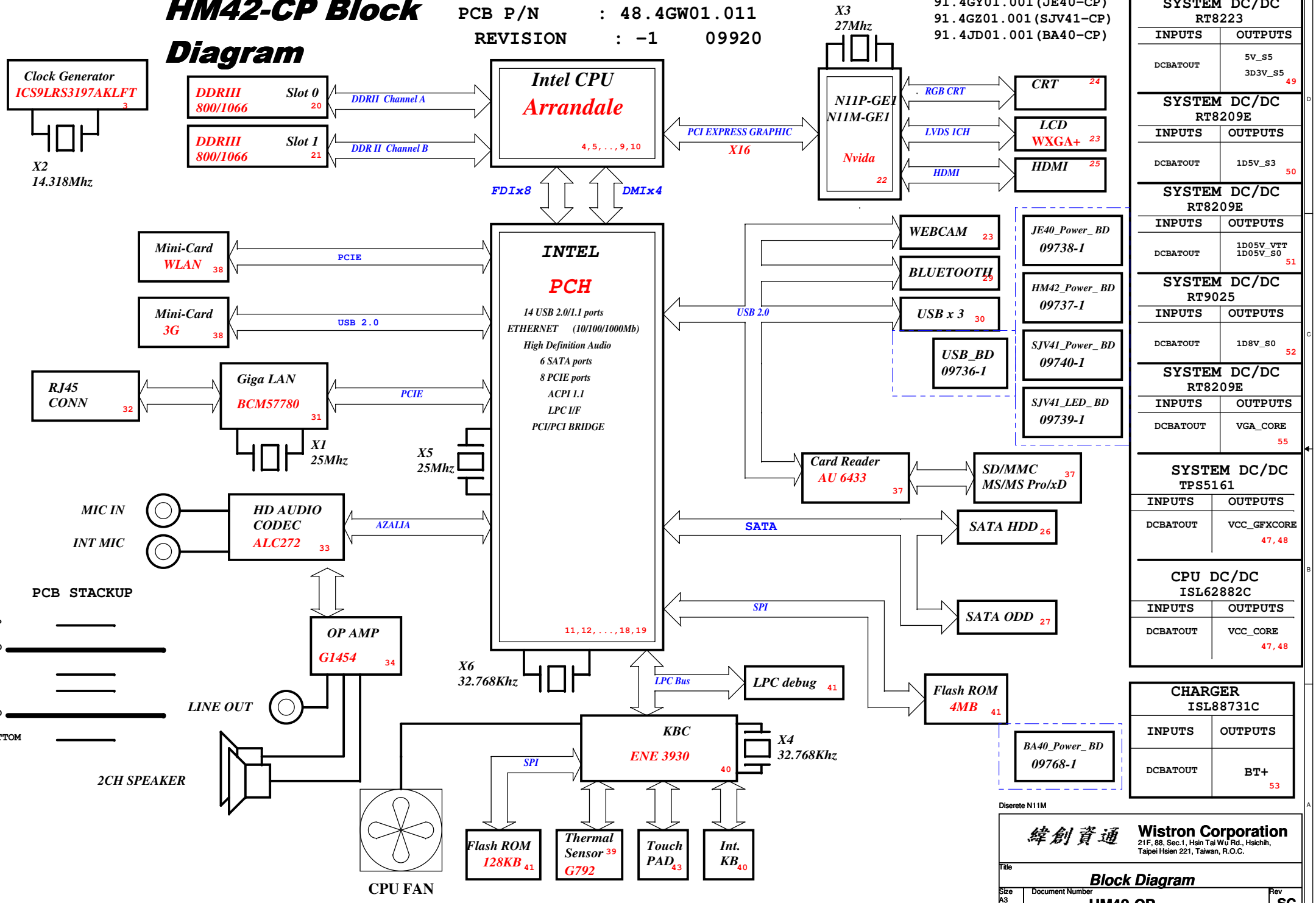
HM42-CP Block Diagram

PCB P/N : 48.4GW01.011
REVISION : -1 09920

Project code: 91.4GW01.001(HM42-CP)
91.4GY01.001(JE40-CP)
91.4GZ01.001(SJV41-CP)
91.4JD01.001(BA40-CP)



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0 51

SYSTEM DC/DC RT9025	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0 52

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 55

SYSTEM DC/DC TPS5161	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 47,48

CPU DC/DC ISL62882C	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

CHARGER ISL88731C	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

Diserete N11M

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

<Variant Name>

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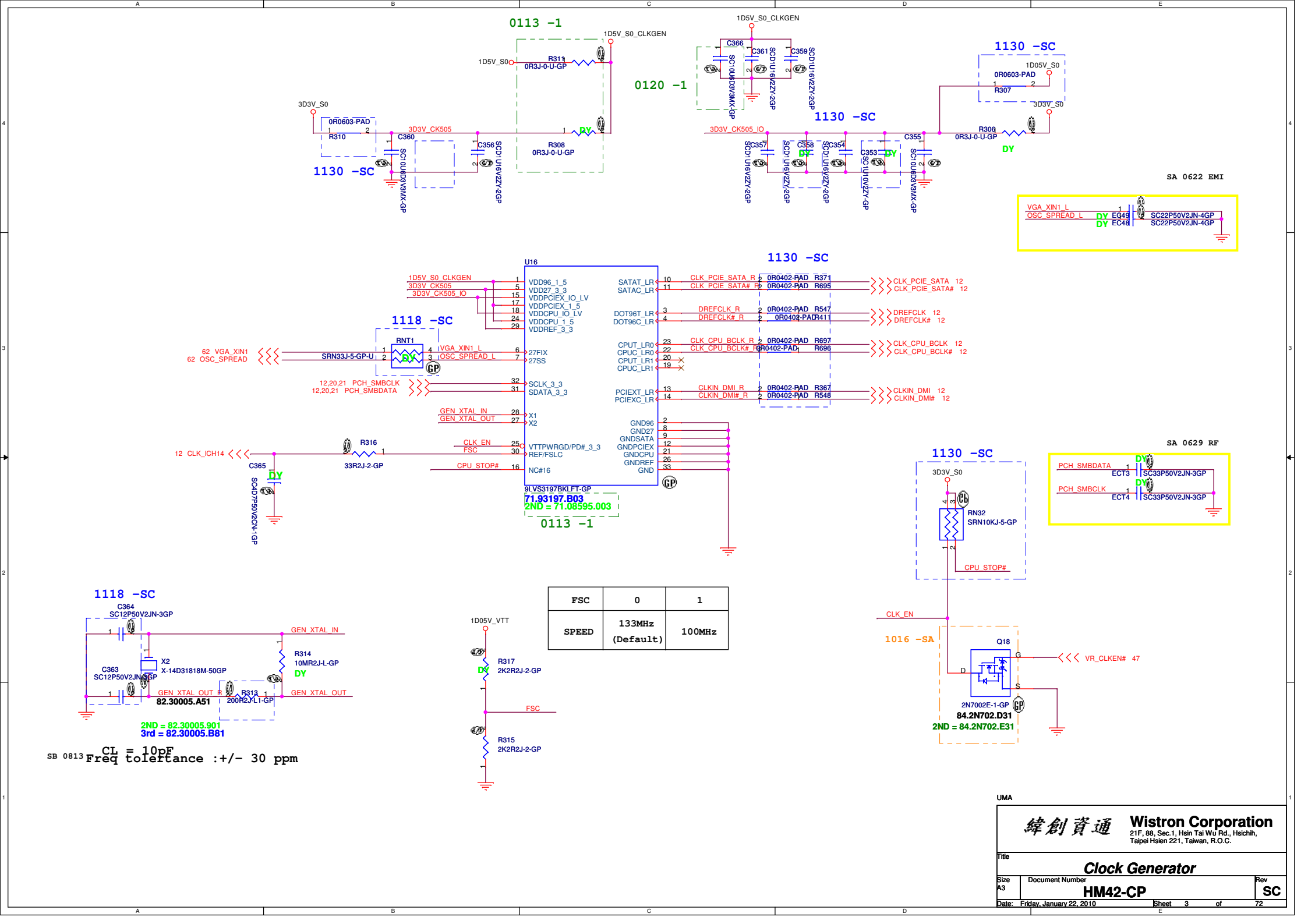
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3D3V_S0
0R0603-PAD
R310
3D3V_CK505
C360
SC10U6D3V3MX-GP
C356
SCD1U16V2ZY-2GP
R308
0R3J-0-U-GP
DY
1130 -SC
0120 -1
C366
C361
C359
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C354
C353
C355
R306
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OSC_SPREAD_L
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EC48
SC22P50V2JN-4GP
U16
1130 -SC
1118 -SC
RNT1
SRN33J-5-GP-U
62 VGA_XIN1
62 OSC_SPREAD
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OSC_SPREAD_L
27FIX
27SS
12,20,21 PCH_SMBCLK
12,20,21 PCH_SMBDATA
SCLK_3_3
SDATA_3_3
GEN_XTAL_IN
GEN_XTAL_OUT
X1
X2
12 CLK_ICH14
R316
33R2J-2-GP
C365
SCAD7P50V2CN-1GP
CLK_EN
FSC
CPU_STOP#
VTTPWRGD/PD#_3_3
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SATAC_LR
DOT96T_LR
DOT96C_LR
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CPUC_LR0
CPUT_LR1
CPUC_LR1
PCIEXT_LR
PCIEXC_LR
GND96
GND27
GNDSATA
GNDPCIEX
GNDCPU
GNDREF
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R695
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R411
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R696
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R367
R548
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CLKIN_DMI# 12
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PCH_SMBCLK
ECT3
ECT4
SC33P50V2JN-3GP
1130 -SC
3D3V_S0
RN32
SRN10KJ-5-GP
CPU_STOP#
CLK_EN
1016 -SA
Q18
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
VR_CLKEN# 47
1118 -SC
C364
SC12P50V2JN-3GP
C363
SC12P50V2JN-3GP
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DY
R313
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3rd = 82.30005.B81
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R317
2K2R2J-2-GP
FSC
R315
2K2R2J-2-GP
FSC
0
1
SPEED
133MHz (Default)
100MHz
SB 0813
CL = 10pF
Freq tolerance :+/- 30 ppm
UMA
緯創資通
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Title
Clock Generator
Size
A3
Document Number
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SC
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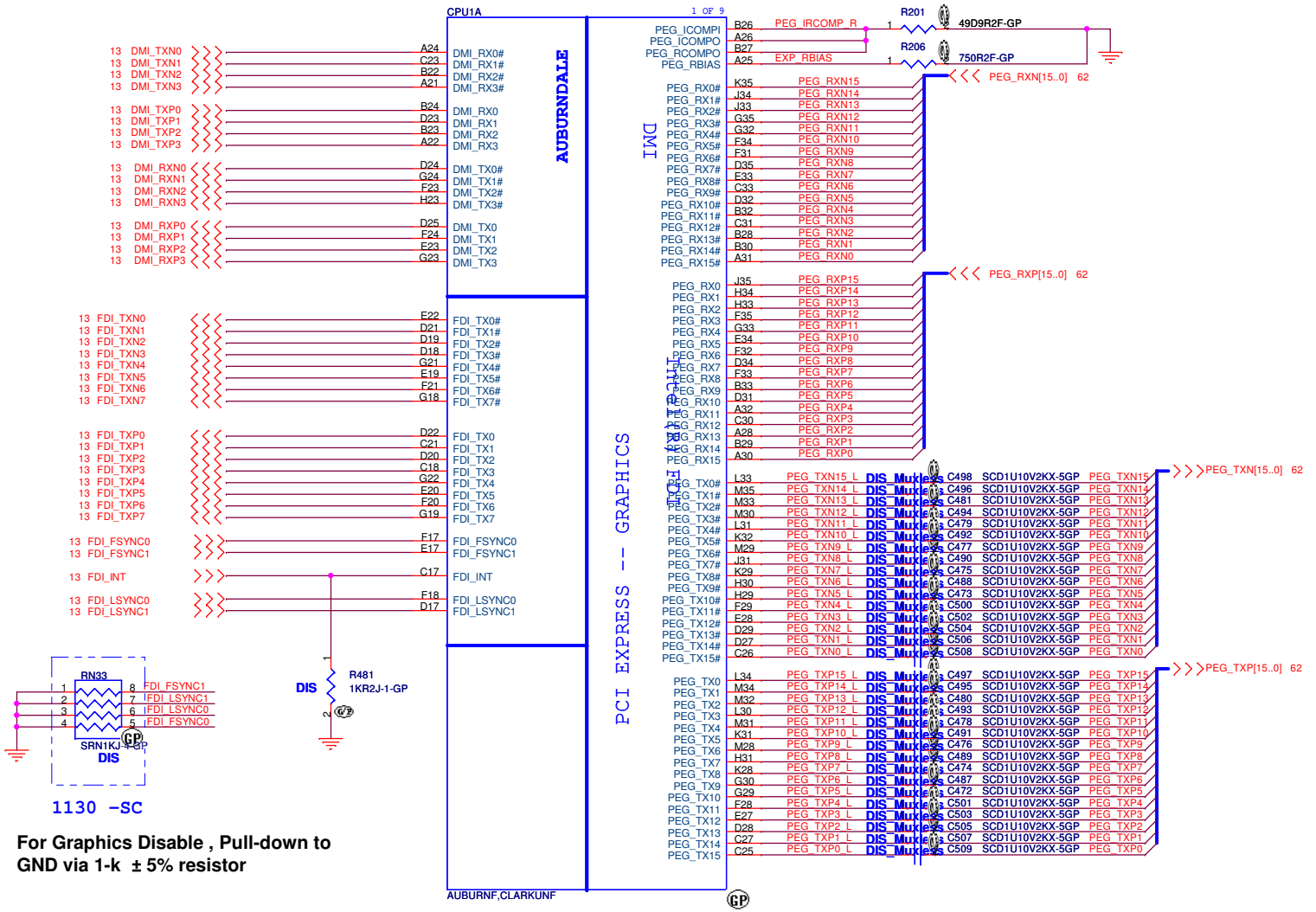

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Title	*CPU (1/7)*
Size A3	Document Number **HM42-CP** Rev **SC**
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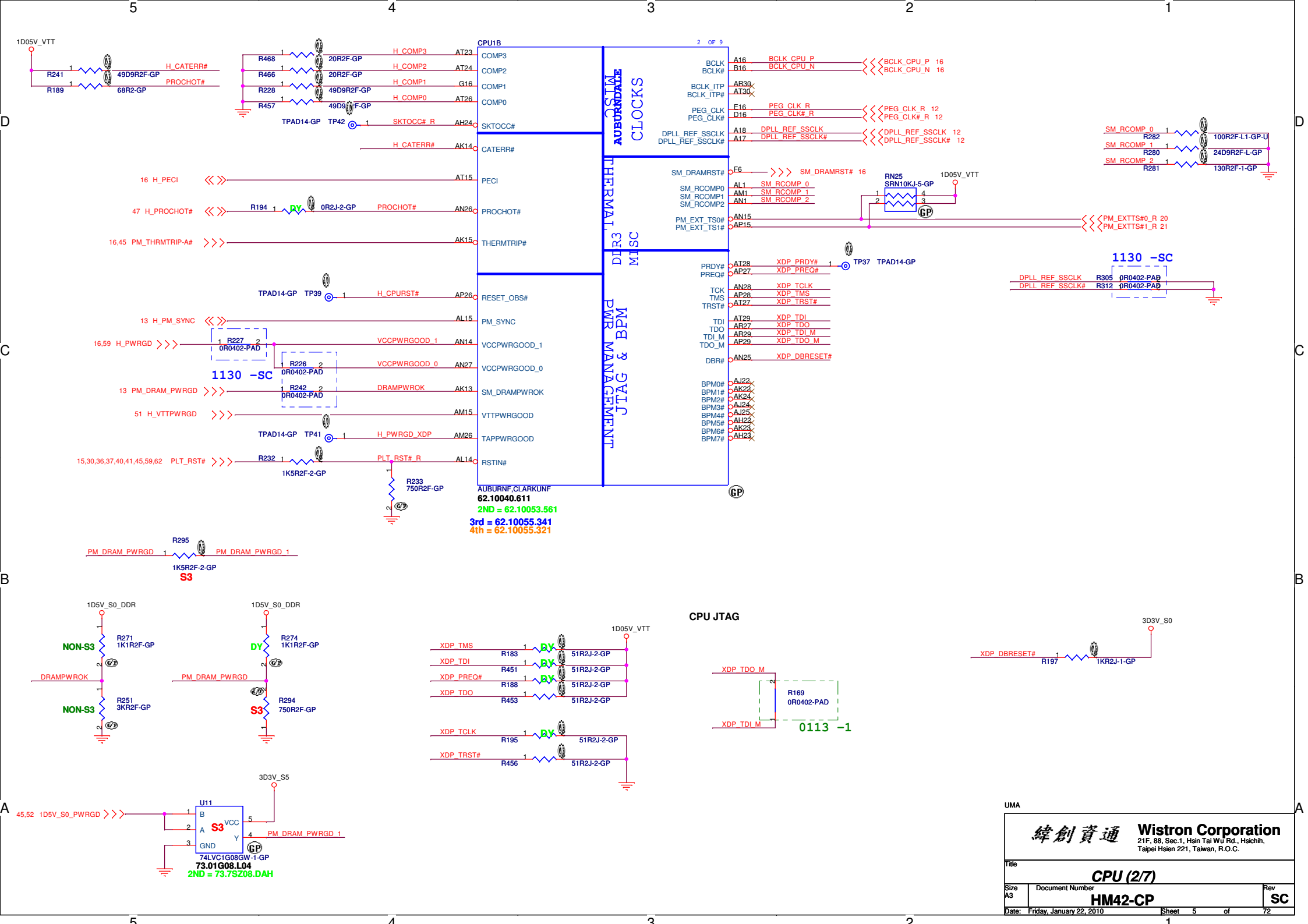
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4th = 62.10055.321
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DPLL_REF_SSCLK#
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SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS0#
PM_EXT_TS1#
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM0#
BPM1#
BPM2#
BPM3#
BPM4#
BPM5#
BPM6#
BPM7#
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XDP_TDO_M
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SM_RCOMP_1
SM_RCOMP_2
PM_EXTTS#0_R
PM_EXTTS#1_R
RN25
SRN10KJ-5-GP
1130 -SC
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PM_DRAM_PWRGD_1
VTTPWRGD
PLT_RST#
S3
NON-S3
DY
GP
3D3V_S0
3D3V_S5
1D05V_S0_DDR
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UMA
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
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CPU (2/7)
Size A3
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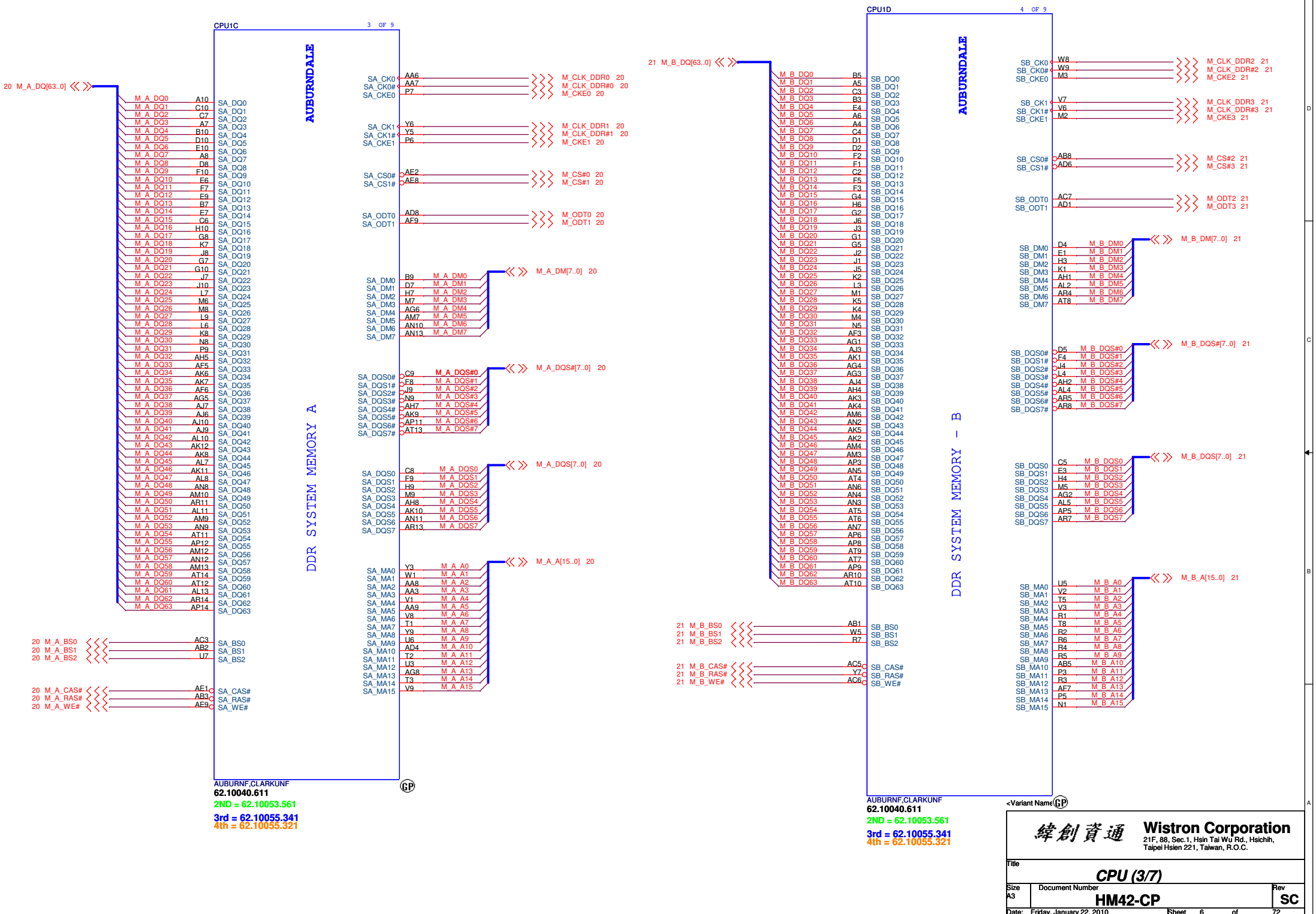
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SA_CK1 Y6 M_CLK_DDR1 20
SA_CK1# Y5 M_CLK_DDR#1 20
SA_CKE1 P6 M_CKE1 20
SA_CS0# AE2 M_CS#0 20
SA_CS1# AE8 M_CS#1 20
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SA_ODT1 AF9 M_ODT1 20
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SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15
M_A_A[15..0] 20
AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321
CPU1D
4 OF 9
AUBURNDALE
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M_B_DQ2 C3 SB_DQ2
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M_B_DQ5 A6 SB_DQ5
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M_B_DQ7 C4 SB_DQ7
M_B_DQ8 D1 SB_DQ8
M_B_DQ9 D2 SB_DQ9
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M_B_DQ28 K5 SB_DQ28
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M_B_DQ63 AT10 SB_DQ63
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21 M_B_WE# AC6 SB_WE#
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SB_CK0# W9 M_CLK_DDR#2 21
SB_CKE0 M3 M_CKE2 21
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M_B_DQS[7..0] 21
SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AF7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15
M_B_A[15..0] 21
AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (3/7)
Size A3
Document Number HM42-CP
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Date: Friday, January 22, 2010
Sheet 6 of 72

VCC_CORE

1130 -SC 0111 -1

C522 C222 C212 C231 C524 C217
C268 C218 C523 C189 C519 C207
C520 C260 C239 C230 C199 C214
C200 C521 C211 C194 C252 C276

SC10U6D3V3MX-GP

PROCESSOR CORE POWER

48A

CPU1F 6 OF 9

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

1130 -SC

1D05V_VTT

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 — VTT0

C275 C565 C541 C291 C543 C292 C267 — SC10U6D3V3MX-GP

DY

1130 -SC

1D05V_VTT

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15 — VTT0

C303 DY SC10U6D3V3MX-GP

C288 SC10U6D3V3MX-GP

+VTT_43 +VTT_44

1130 -SC

1D05V_VTT

R677 R678 — 0R0402-PAD

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

CPU VIDS

PSI# AN33 — PSI# 47

VID0 AK35 H_VID0
VID1 AK33 H_VID1
VID2 AK34 H_VID2
VID3 AL35 H_VID3
VID4 AL33 H_VID4
VID5 AM33 H_VID5
VID6 AM35 H_VID6

H_VID[6..0] 47

PROC_DPRSLPVR AM34 — PM_DPRSLPVR 47

VTT_SELECT G15 H_VTTVID1 — TP53 TPAD14-GP

Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V

SENSE LINES

ISENSE AN35 — IMVP_IMON 47

VCC_CORE

R129 100R2F-L1-GP-U

VCC_SENSE AJ34 — VCC_SENSE 47
VSS_SENSE AJ35 — VSS_SENSE 47

R128 100R2F-L1-GP-U

VTT_SENSE B15 — VTT_SENSE 51
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT — TP51 TPAD14-GP

AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561 3rd = 62.10055.341 4th = 62.10055.321

<Variant Name>

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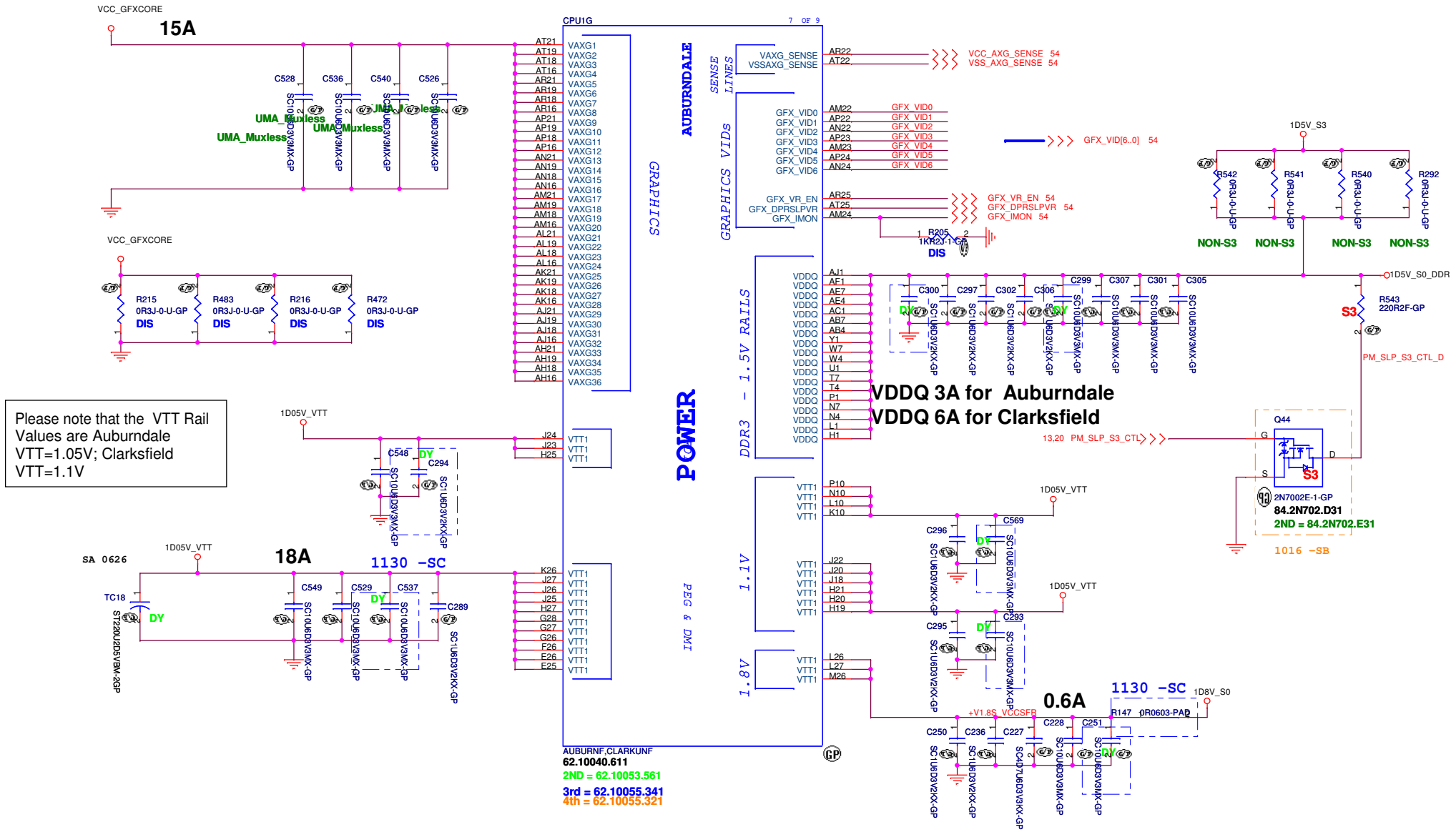
Title: CPU (4/7)

Size: Custom | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 7 of 72



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (5/7)***	
Size A3	Document Number **HM42-CP**	Rev **SC**
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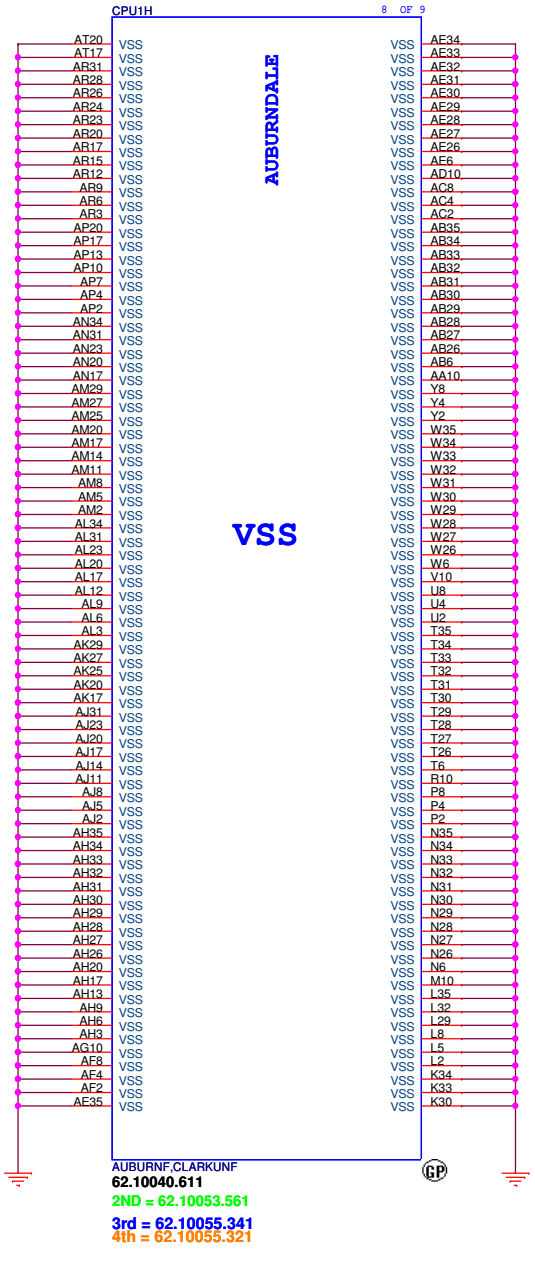

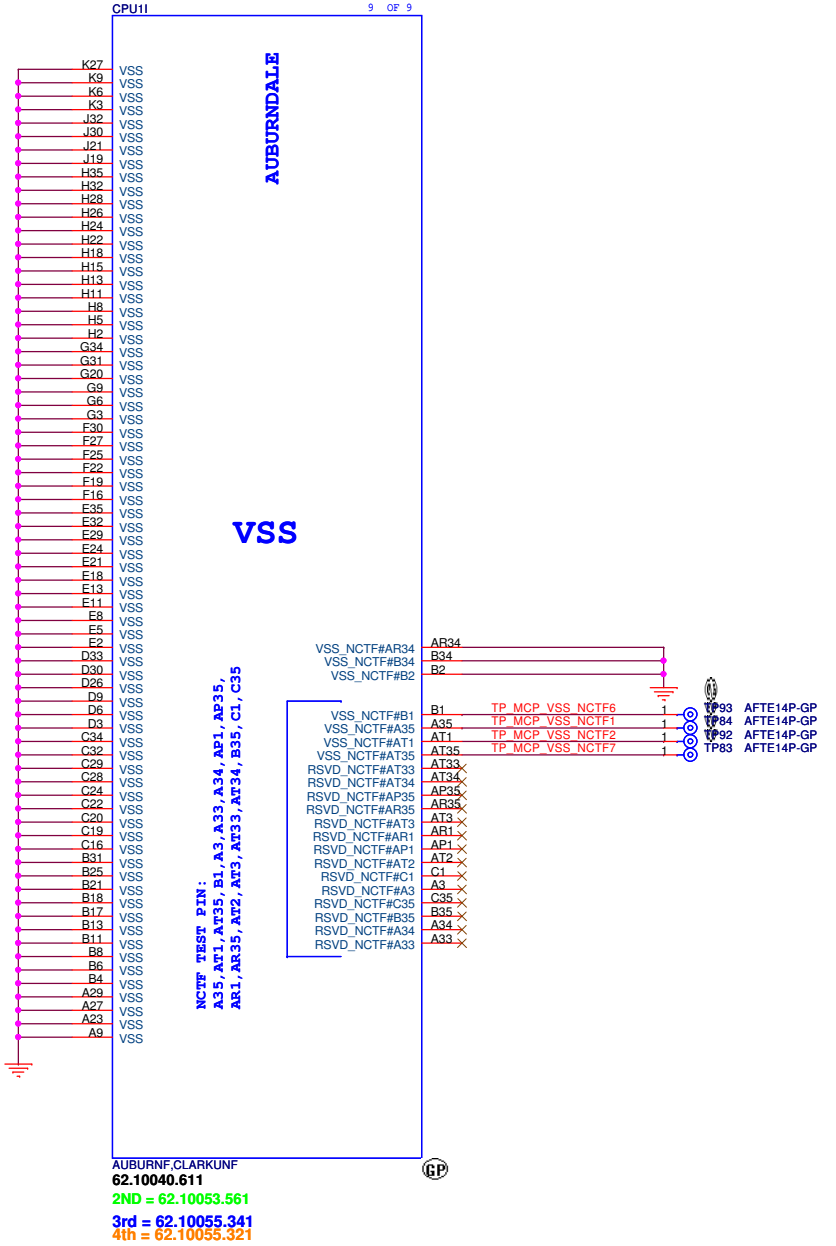

<Variant Name>

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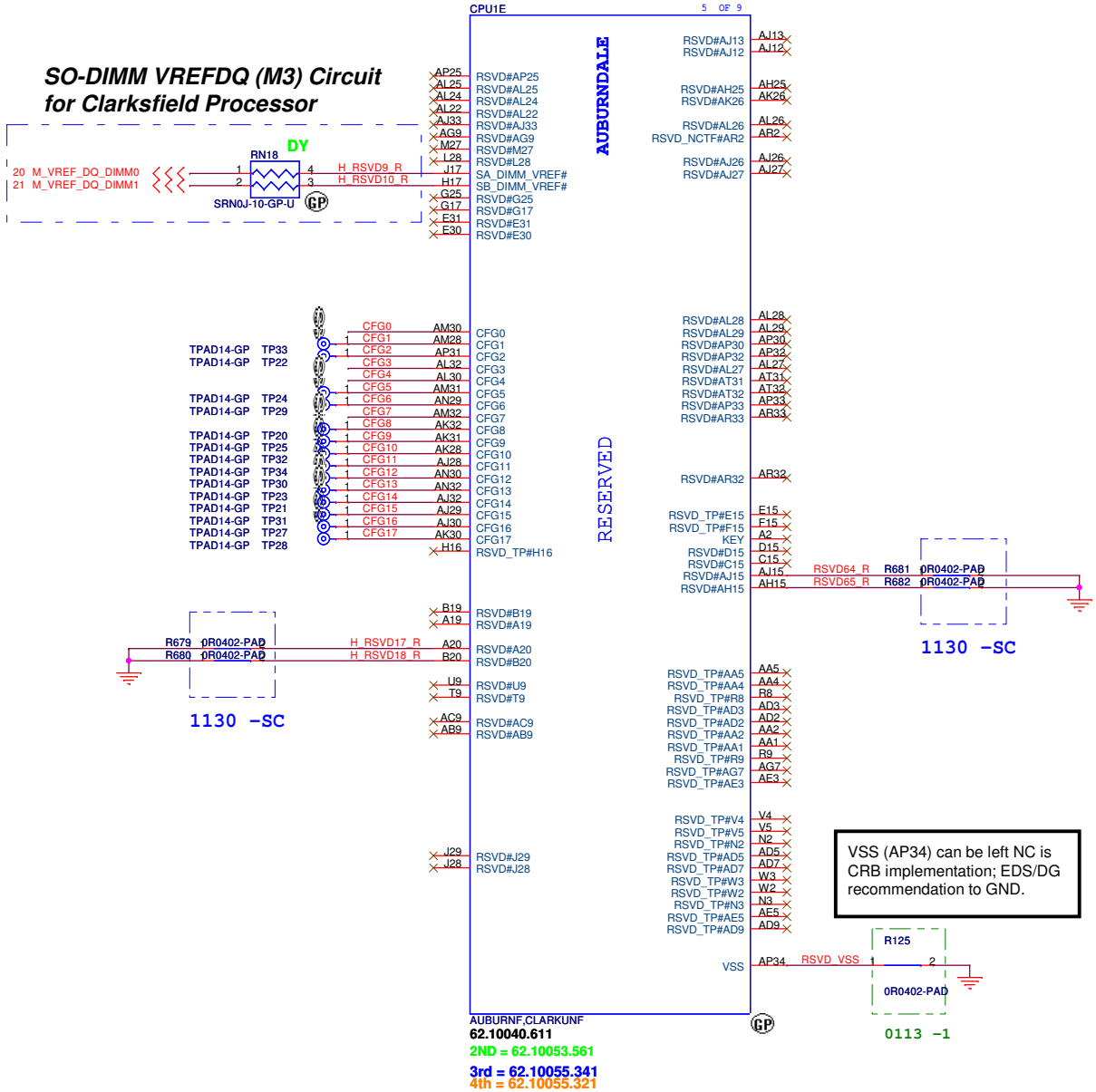
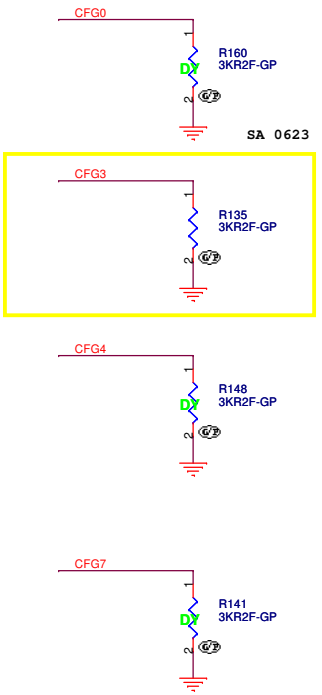
Title: ***CPU (6/7)***

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 9 of 72





Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Variant Name>

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Title: CPU (7/7)

Size	Document Number	Rev
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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

ICH_RTCX1 — R482 10MR2J-L-GP — ICH_RTCX2
X6 — X-32D768KHZ-34GPU
C547 SC6P50V2CN-1GP — C544 SC6P50V2CN-1GP
82.30001.661
2nd = 82.30001.B21
CL = 7pF
Freq tolertance :+/- 20 ppm
1202 -SC

RTC_AUX_S5 — RN55 SRN20KJ-GP-U — C527 SC1U6D3V2KX-GP
RTC_AUX_S5 — R470 1MR2J-1-GP — SM_INTRUDER#
R475 330KR2F-L-GP — ICH_INTVRMEN

SA 0629 RF
ACZ_RST# DY ECT5 SC33P50V2JN-3GP
ACZ_SYNC DY ECT7 SC33P50V2JN-3GP
ACZ_BIT_CLK DY ECT6 SC33P50V2JN-3GP
ACZ_SDATAOUT DY ECT8 SC33P50V2JN-3GP

C530 SC1U6D3V2KX-GP — G59 GAP-OPEN
SRTCRST# new signal Pin

32 ACZ_RST#_AUDIO — R455 10R2J-2-GP — ACZ_RST#
32 ACZ_SYNC_AUDIO — R461 10R2J-2-GP — ACZ_SYNC
32 ACZ_BITCLK_AUDIO — R458 10R2J-2-GP — ACZ_BIT_CLK
32 ACZ_SDATAOUT_AUDIO — R463 33R2J-2-GP — ACZ_SDATAOUT
1117 -SC

SIV fail when stuff 10-ohm,
fine tune 33-ohm for solving
33-ohm is required for intel recommend,
real value base on fine tune result

NO REBOOT STRAP
3D3V_S0 — R516 DY 1KR2J-1-GP — ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SA 0709
For after PCH stepping B3,have to DY,

1113 -SC
3D3V_S5
PCH_JTAG_TMS — DY R512 200R2J-L1-GP
PCH_JTAG_TDO — DY R509 200R2J-L1-GP
PCH_JTAG_TDI — DY R513 200R2J-L1-GP
PCH_JTAG_RST# — DY R235 10KR2J-3-GP
PCH_JTAG_TMS — DY R511 100R2J-2-GP
PCH_JTAG_TDO — DY R510 100R2J-2-GP
PCH_JTAG_TDI — DY R514 100R2J-2-GP
PCH_JTAG_RST# — DY R240 51R2F-2-GP
PCH_JTAG_TCK — R515 51R2F-2-GP
When unused all JTAG pins may be NC

PCH1A — 1 OF 10

ICH_RTCX1	B13	RTCX1	RTC
ICH_RTCX2	D13	RTCX2	
ICH_RTCRST#	C14	RTCRST#	
SRTCRST#	D17	SRTCRST#	
SM_INTRUDER#	A16	INTRUDER#	
ICH_INTVRMEN	A14	INTVRMEN	
ACZ_BIT_CLK	A30	HDA_BCLK	IHDA
ACZ_SYNC	D29	HDA_SYNC	
32 ACZ_SPKR	P1	SPKR	
ACZ_RST#	C30	HDA_RST#	
32 ACZ_SDATAIN0	G30	HDA_SDIN0	
TPAD14-GP TP40 — ACZ_SDATAIN1	F30	HDA_SDIN1	
TPAD14-GP TP38 — HDA_SDIN2	E32	HDA_SDIN2	
HM4-CP SA	F32	HDA_SDIN3	
ACZ_SDATAOUT	B29	HDA_SDO	
1130 -SC			
40 ME_UNLOCK# — R182 0R0402-PAD	H32	HDA_DOCK_EN#/GPIO33	
R187 8K2R2J-3-GP DY	J30	HDA_DOCK_RST#/GPIO13	
PCH_JTAG_TCK	M3	JTAG_TCK	JTAG
PCH_JTAG_TMS	K3	JTAG_TMS	
PCH_JTAG_TDI	K1	JTAG_TDI	
PCH_JTAG_TDO	J2	JTAG_TDO	
PCH_JTAG_RST#	J4	TRST#	
0113 -1			
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK: No series resistor required if routing length is 1.5"-6.5"			
41 PCH_SPI_CS#0 — PCH_SPI_CS#0	BA2	SPI_CLK	SPI
41 PCH_SPI_MOSI — PCH_SPI_MOSI	AV3	SPI_CS0#	
41 PCH_SPI_CLK — PCH_SPI_CLK	AY3	SPI_CS1#	
RN81 SRN15J-GP	AY1	SPI_MOSI	
41 SPI_MOSO_R	AV1	SPI_MISO	
IBEXPEAK-M-GP-NF			

FWH0/LAD0	D33	LPC_LAD0 40,41	LPC
FWH1/LAD1	B33	LPC_LAD1 40,41	
FWH2/LAD2	C32	LPC_LAD2 40,41	
FWH3/LAD3	A32	LPC_LAD3 40,41	
FWH4/LFRAME#	C34	LPC_LFRAME# 40,41	
LDRQ0#	A34		
LDRQ1#/GPIO23	F34	PCH_GPIO23 — TP35 TPAD14-GP	
SERIRQ	AB9	INT_SERIRQ — INT_SERIRQ 16,40	
SATA0RXN	AK7	SATA_RXN0 26	SATA
SATA0RXP	AK6	SATA_RXP0 26	
SATA0TXN	AK11	SATA_TXN0 26	
SATA0TXP	AK9	SATA_TXP0 26	
SATA1RXN	AH6		
SATA1RXP	AH5		
SATA1TXN	AH9		
SATA1TXP	AH8		
SATA2RXN	AE11		
SATA2RXP	AF9		
SATA2TXN	AF7		
SATA2TXP	AF6		
SATA3RXN	AH3		
SATA3RXP	AH1		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	AD9	SATA_RXN4 27	
SATA4RXP	AD8	SATA_RXP4 27	
SATA4TXN	AD6	SATA_TXN4 27	
SATA4TXP	AD5	SATA_TXP4 27	
SATA5RXN	AD3		
SATA5RXP	AD1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	AF16		
SATAICOMPI	AF15	SATAICOMP — R219 37D4R2F-GP — 1D05V_S0	
SATALED#	T3	SATA_LED# — SATA_LED# 16,44	
SATA0GP/GPIO21	Y9	SATA_DET#0_R	
SATA1GP/GPIO19	V1	SATA_DET#1_R	

HDD
ODD

PCH 1 stuff 71.0IBEX.G0U

PCH Strapping

SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required

3D3V_S0 — R250 DY 8K2R2J-3-GP — SPI_MOSI_R

RTC_AUX_S5 — R298 0R3J-0-U-GP — RTC_PWR_L — C330 SC1U10V2ZY-GP
3D3V_AUX_S5 — D10 BAS40CW-GP — RTC_PWR — R297 1KR2J-1-GP — RTC_BAT
RTC1 MLX-CON2-13-GP
83.00040.E81
2nd = 83.00040.M81
3rd = 83.00040.R81
20.F1035.002
2nd = 20.F0772.002
3rd = 21.D0300.102
4th = 20.F1729.002

16 PCH_GPIO48 — SATA_DET#0_R — SATA_DET#1_R — PCH_GPIO48 — RN28 SRN10KJ-7GP — 3D3V_S0

83.00040.Q81 is ROHS parts
83.00040.R81 is Halogens free Part
arrange qual in Eng SKU
1130 -SC
0113 -1

UMA

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Title	PCH (1/9)	
Size A3	Document Number HM42-CP	Rev SC
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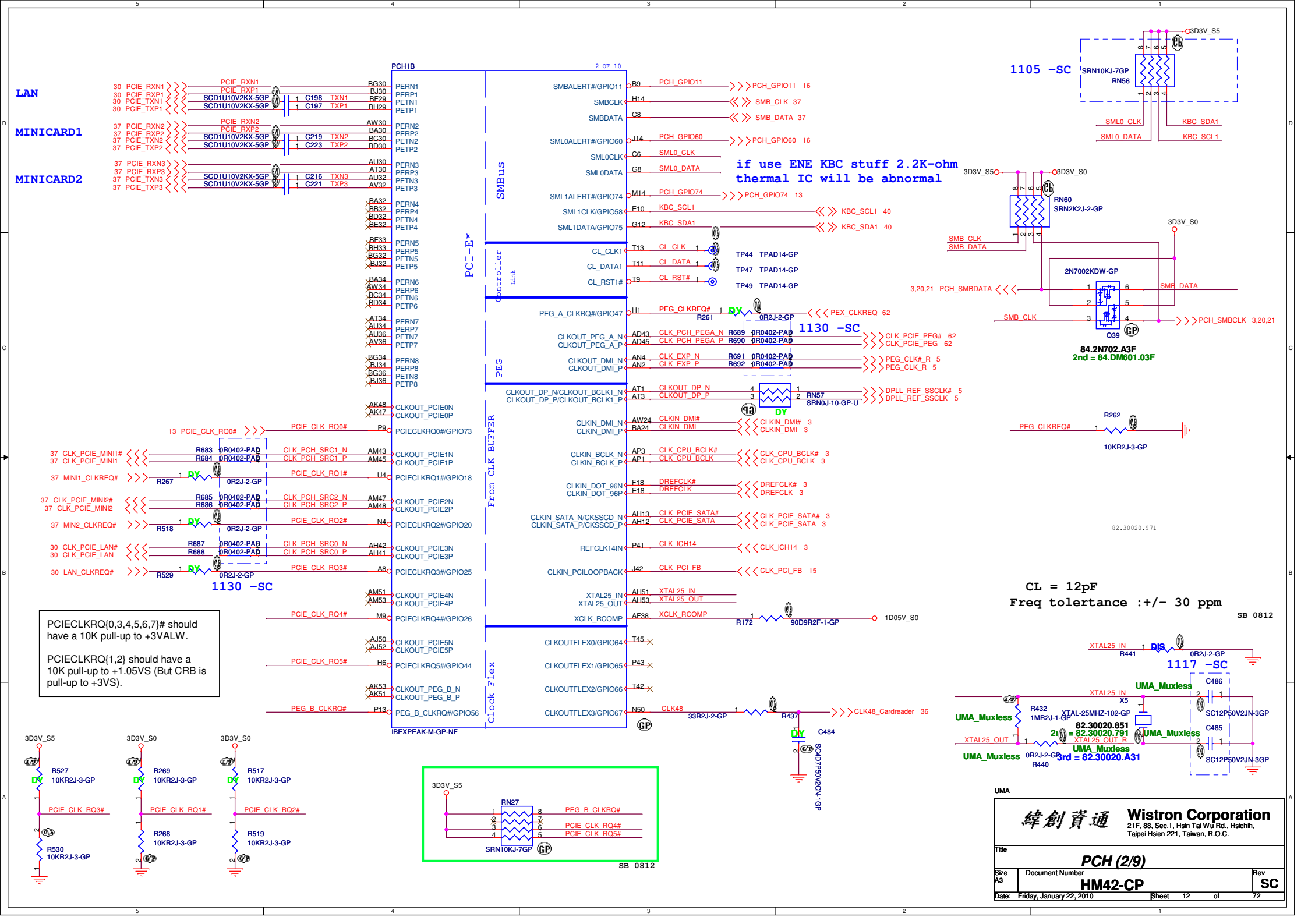
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
if use ENE KBC stuff 2.2K-ohm thermal IC will be abnormal
1105 -SC
1130 -SC
1130 -SC
1117 -SC
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
CL = 12pF
Freq tolerance :+/- 30 ppm
SB 0812
SB 0812
84.2N702.A3F
2nd = 84.DM601.03F
82.30020.971
82.30020.851
2nd = 82.30020.791
3rd = 82.30020.A31
UMA
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PCH (2/9)
HM42-CP
Rev SC
Date: Friday, January 22, 2010
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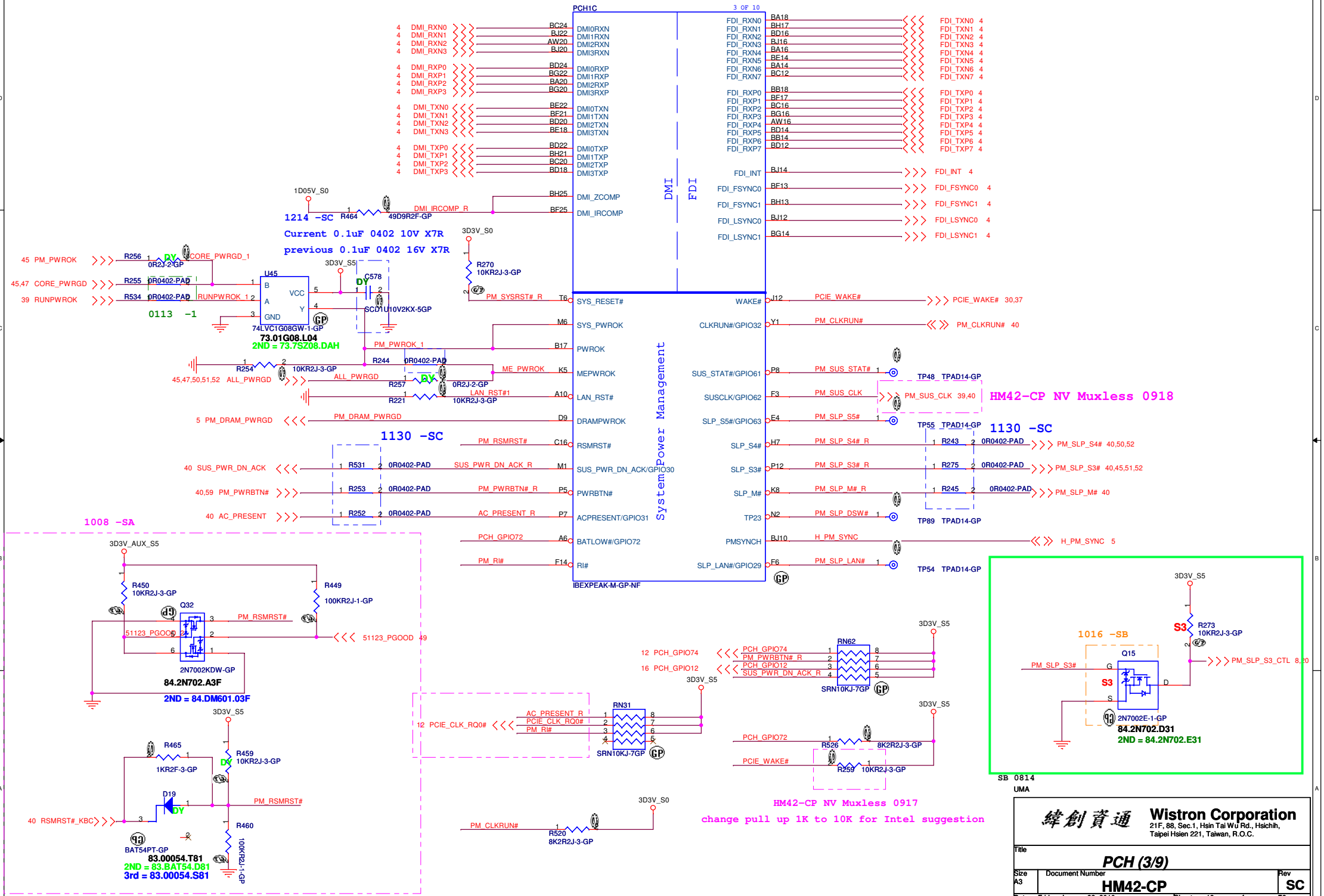
PCH1C
3 OF 10
DMI
FDI
System Power Management
IBEXPEAK-M-GP-NF
DMI0RXN
DMI1RXN
DMI2RXN
DMI3RXN
DMI0RXP
DMI1RXP
DMI2RXP
DMI3RXP
DMI0TXN
DMI1TXN
DMI2TXN
DMI3TXN
DMI0TXP
DMI1TXP
DMI2TXP
DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7
FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
SYS_RESET#
SYS_PWROK
PWROK
MEPWROK
LAN_RST#
DRAMPWROK
RSMRST#
SUS_PWR_DN_ACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN#/GPIO29
1214 -SC
Current 0.1uF 0402 10V X7R
previous 0.1uF 0402 16V X7R
1130 -SC
1008 -SA
0113 -1
HM42-CP NV Muxless 0918
1130 -SC
1016 -SB
HM42-CP NV Muxless 0917
change pull up 1K to 10K for Intel suggestion
SB 0814
UMA
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.00054.S81
SRN10KJ-7GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (3/9)
Size A3
Document Number HM42-CP
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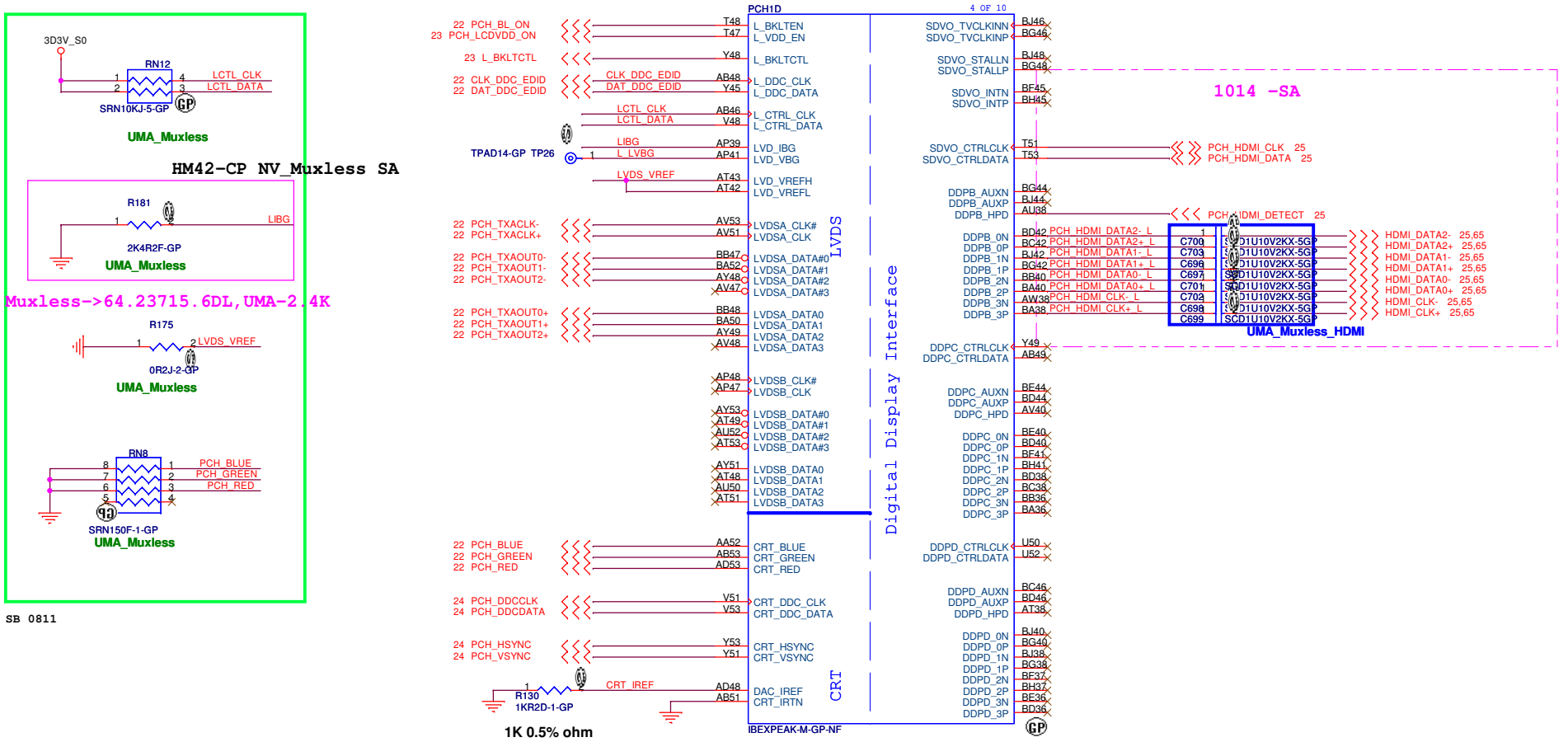

<Core Design>

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Title: PCH (4/9)

Size: A3 | Document Number: HM42-CP | Rev: SC

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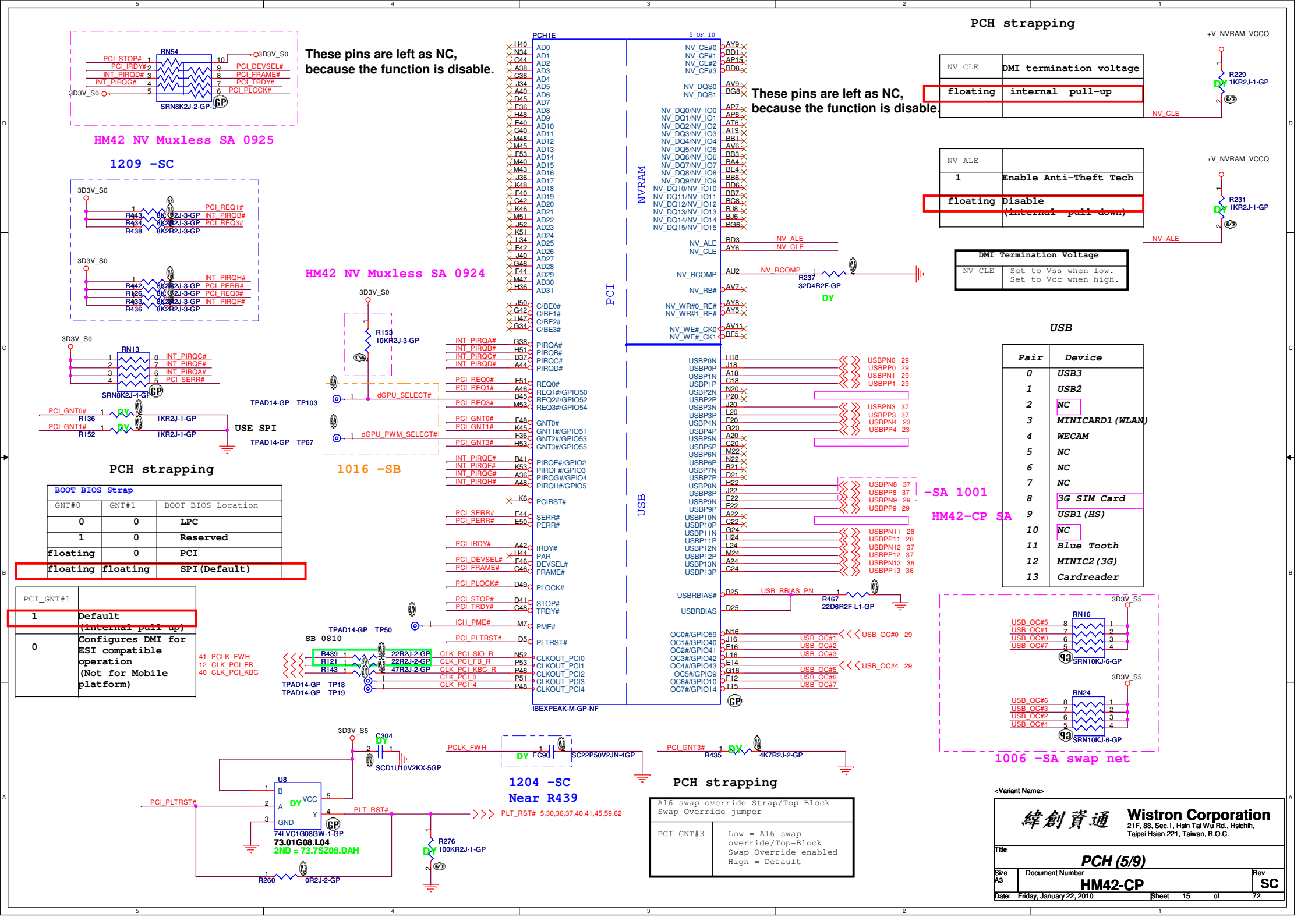
These pins are left as NC, because the function is disable.
HM42 NV Muxless SA 0925
1209 -SC
HM42 NV Muxless SA 0924
1016 -SB
These pins are left as NC, because the function is disable.
PCH strapping
NV_CLE | DMI termination voltage
floating | internal pull-up
NV_ALE
1 | Enable Anti-Theft Tech
floating | Disable (internal pull down)
DMI Termination Voltage
NV_CLE | Set to Vss when low. Set to Vcc when high.
USB
Pair | Device
0 | USB3
1 | USB2
2 | NC
3 | MINICARD1 (WLAN)
4 | WECAM
5 | NC
6 | NC
7 | NC
8 | 3G SIM Card
9 | USB1 (HS)
10 | NC
11 | Blue Tooth
12 | MINIC2 (3G)
13 | Cardreader
-SA 1001
HM42-CP SA
1006 -SA swap net
PCH strapping
BOOT BIOS Strap
GNT#0 | GNT#1 | BOOT BIOS Location
0 | 0 | LPC
1 | 0 | Reserved
floating | 0 | PCI
floating | floating | SPI(Default)
USE SPI
PCI_GNT#1
1 | Default (internal pull up)
0 | Configures DMI for ESI compatible operation (Not for Mobile platform)
SB 0810
1204 -SC
Near R439
PCH strapping
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled
High = Default
PCH1E
IBEXPEAK-M-GP-NF
NVRAM
PCI
USB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
PCH (5/9)
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Document Number
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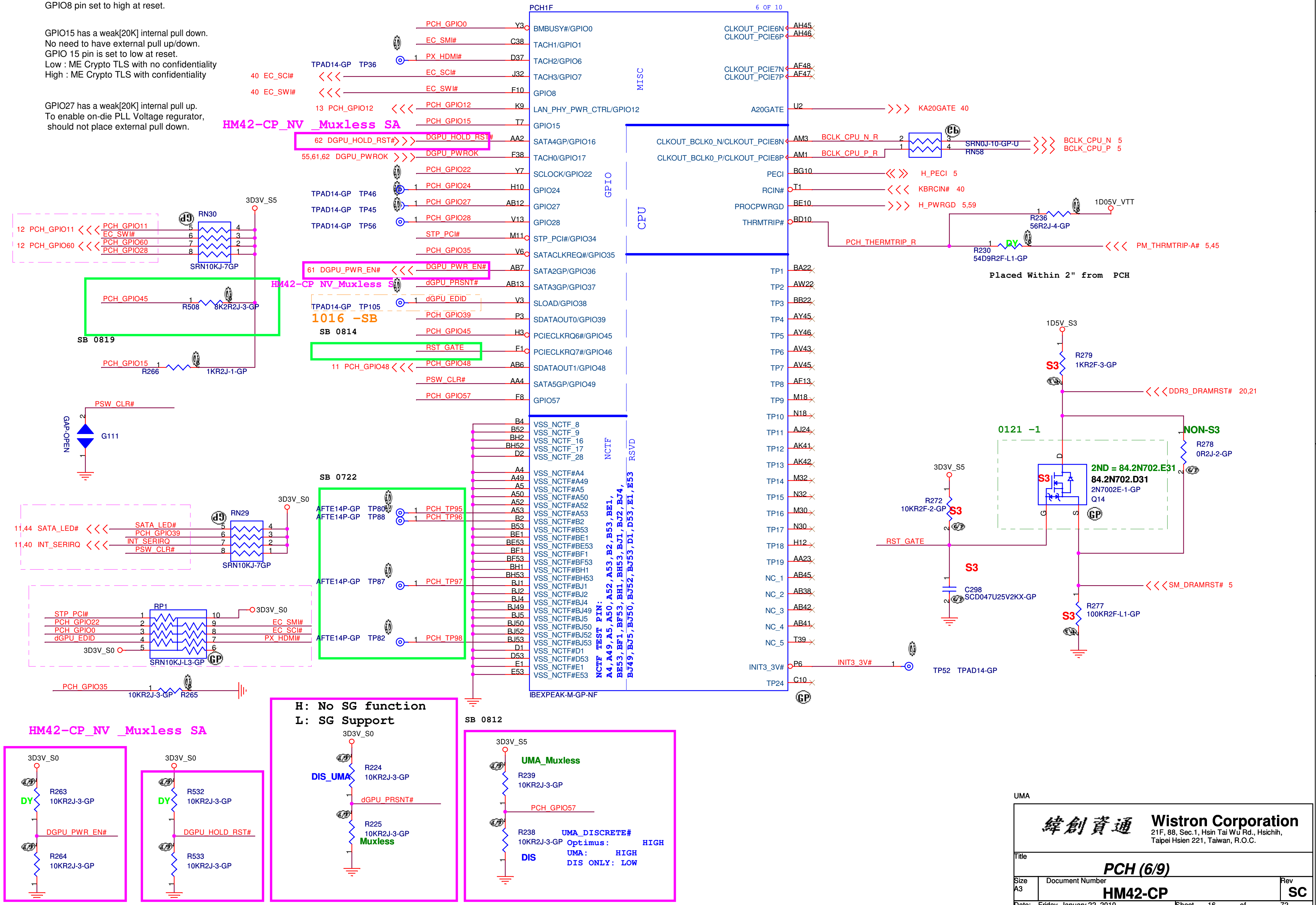
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH (6/9)		
Size: A3	Document Number: HM42-CP	Rev: SC
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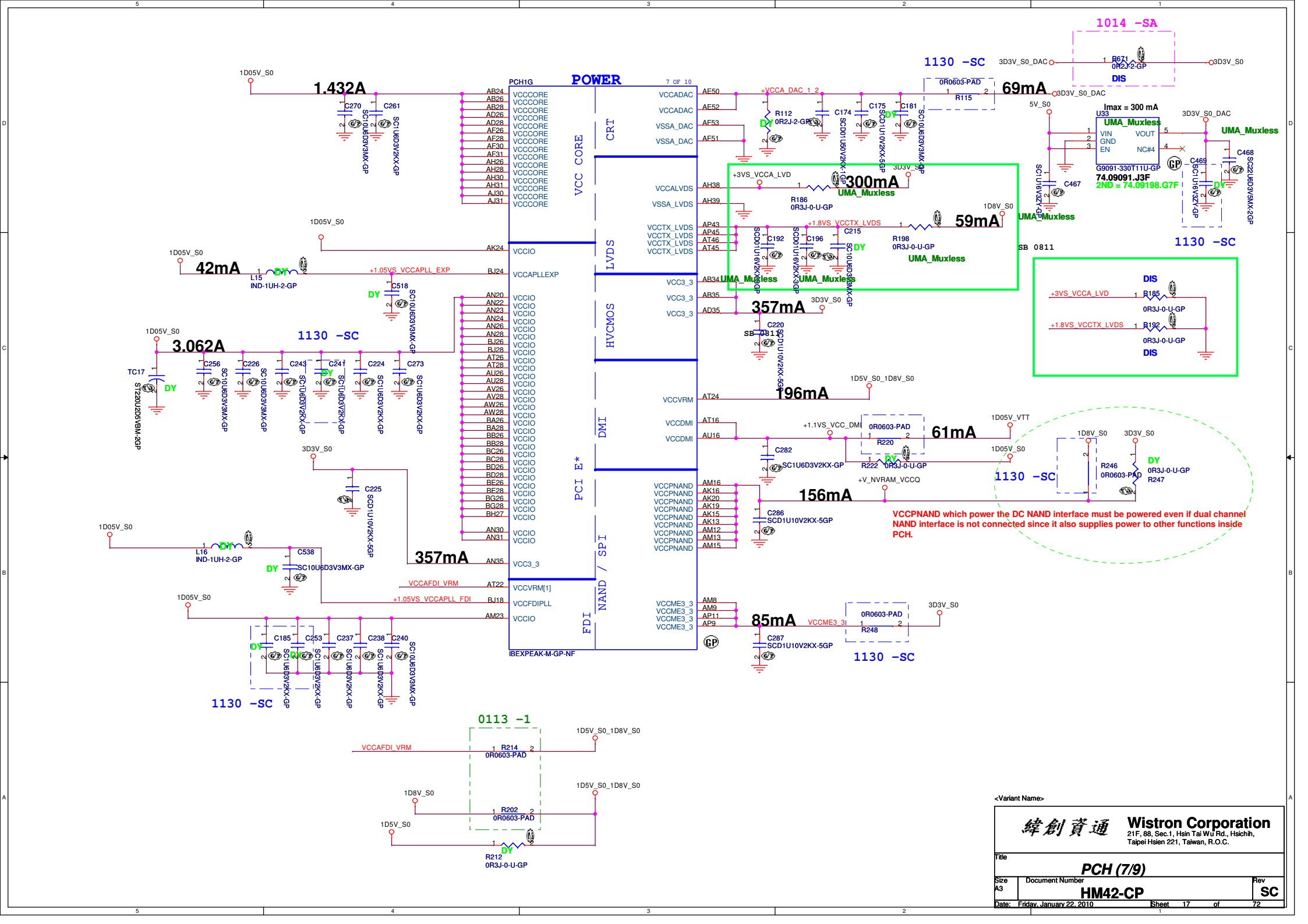
POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
357mA
1130 -SC
1014 -SA
0113 -1
UMA_Muxless
DY
DIS
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
IBEXPEAK-M-GP-NF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (7/9)
Size A3
Document Number HM42-CP
Rev SC
Date: Friday, January 22, 2010
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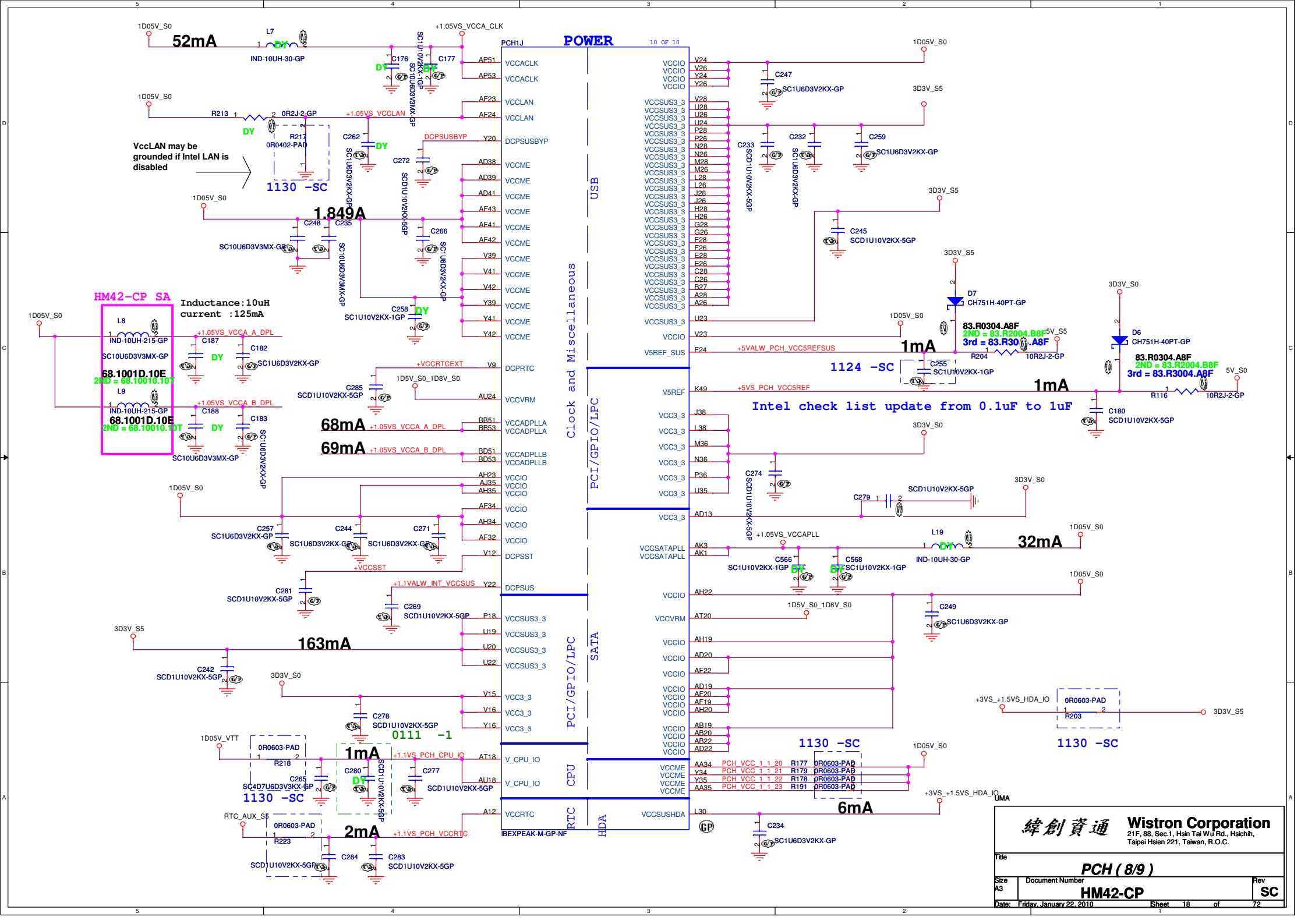
POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
HM42-CP SA
Inductance:10uH
current :125mA
VccLAN may be grounded if Intel LAN is disabled
1130 -SC
1.849A
52mA
68mA
69mA
163mA
1mA
2mA
6mA
32mA
0111 -1
Intel check list update from 0.1uF to 1uF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number
HM42-CP
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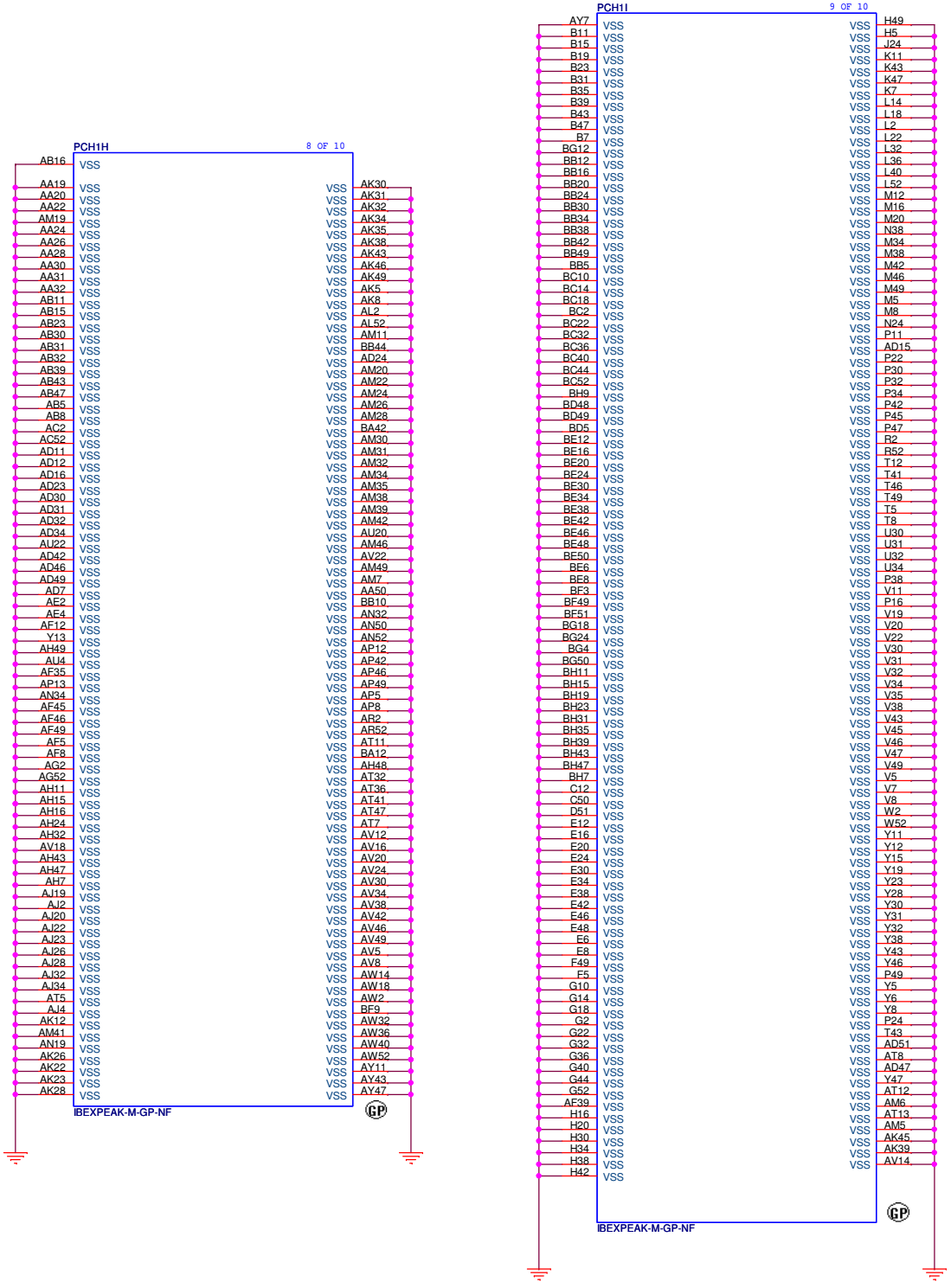

<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (9/9)**

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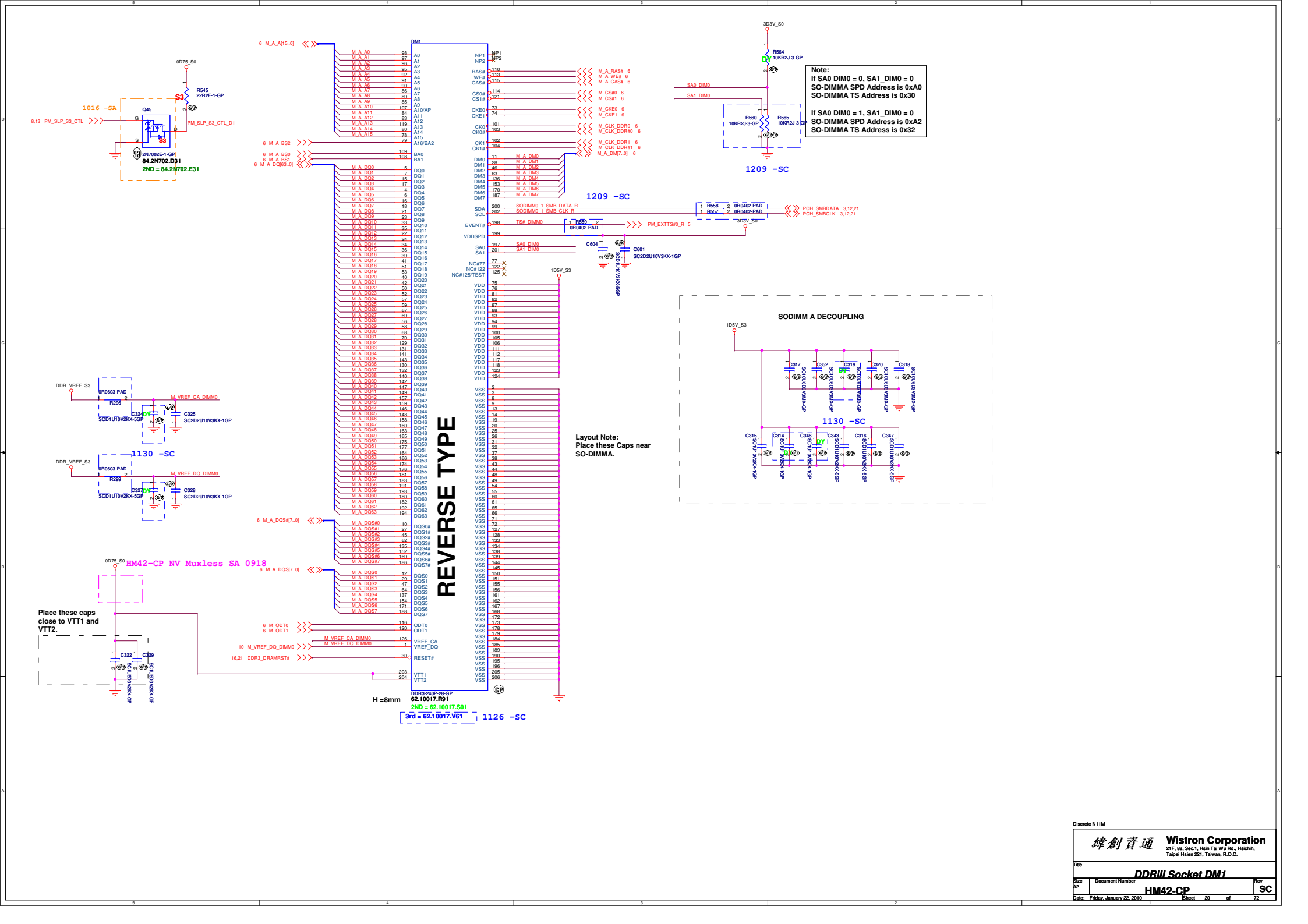
DM1
REVERSE TYPE
DDR3-240P-28-GP
62.10017.R91
2ND = 62.10017.S01
3rd = 62.10017.V61
1126 -SC
H =8mm
1209 -SC
1130 -SC
1016 -SA
HM42-CP NV Muxless SA 0918
Q45
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
Diserete N11M
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size A2
Document Number HM42-CP
Rev SC
Date: Friday, January 22, 2010
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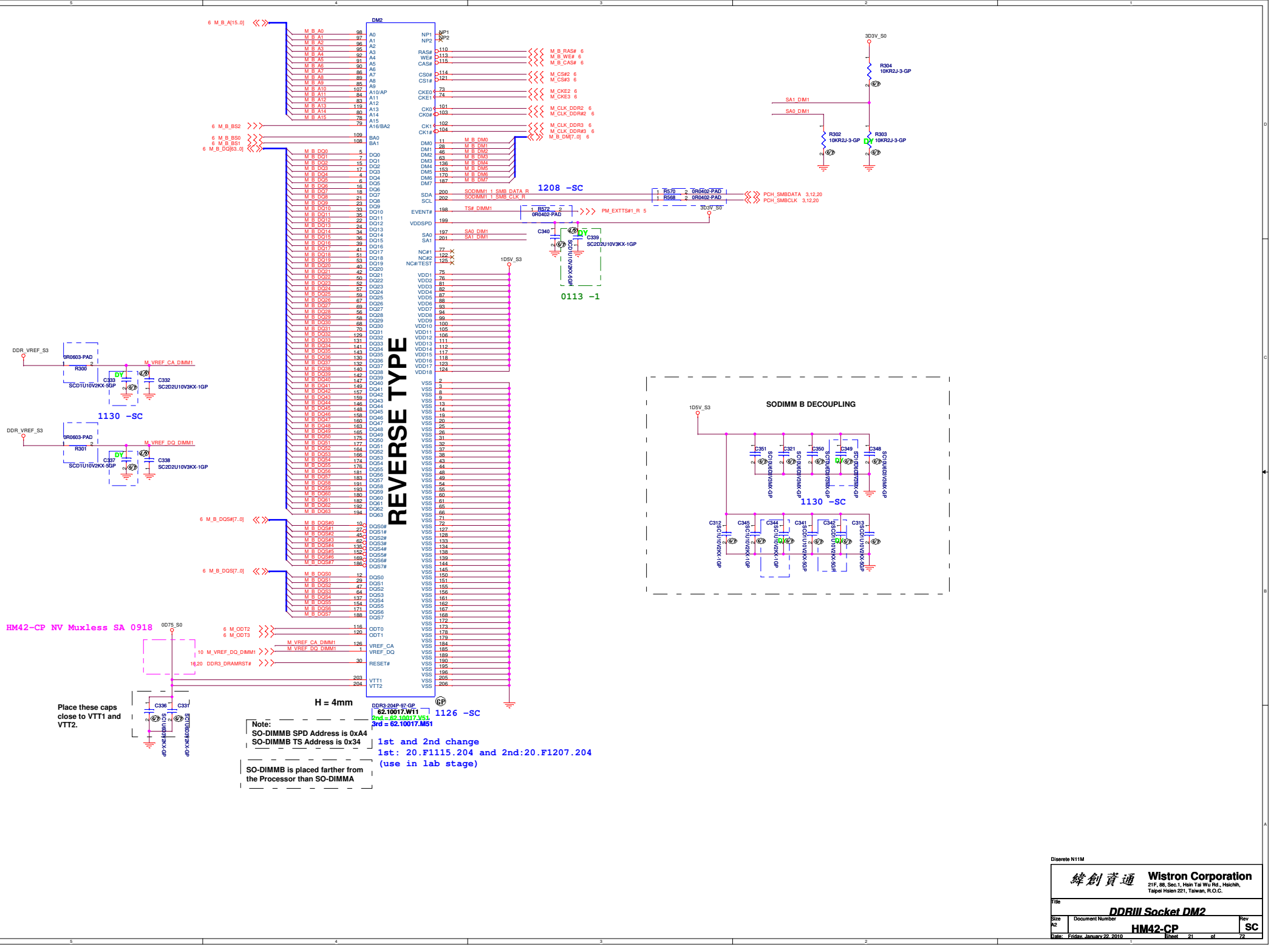
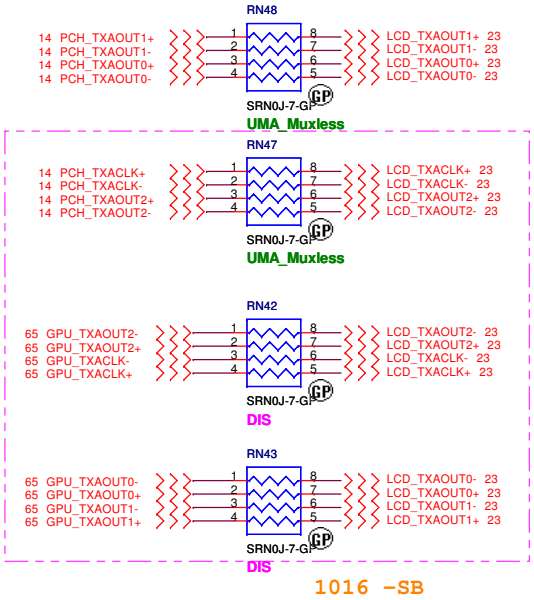
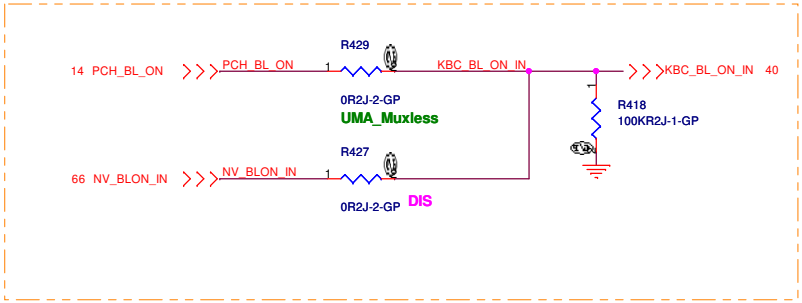
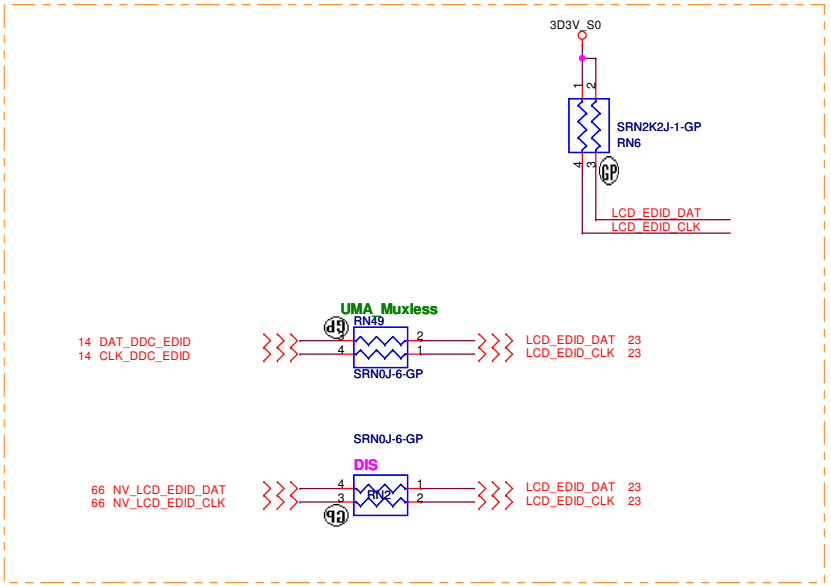
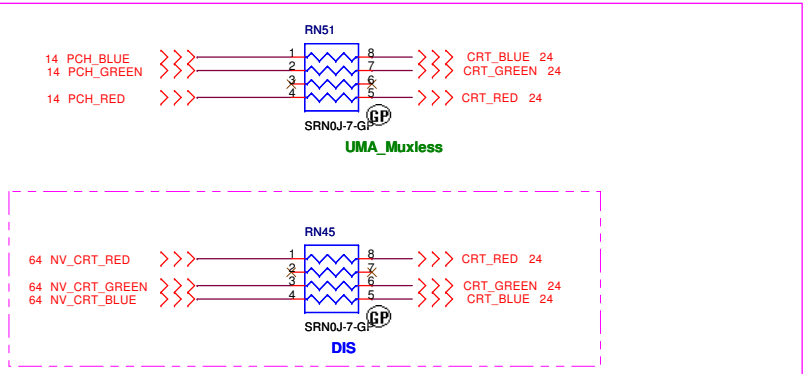

DM2
REVERSE TYPE
DDR3-204P-97-GP
62.10017.W11
2nd = 62.10017.V51
3rd = 62.10017.M51
1126 -SC
1208 -SC
0113 -1
1130 -SC
1130 -SC
SODIMM B DECOUPLING
HM42-CP NV Muxless SA 0918
H = 4mm
Place these caps close to VTT1 and VTT2.
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
1st and 2nd change
1st: 20.F1115.204 and 2nd:20.F1207.204
(use in lab stage)
Diserete N11M
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII Socket DM2
HM42-CP
SC
Friday, January 22, 2010









UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Function***

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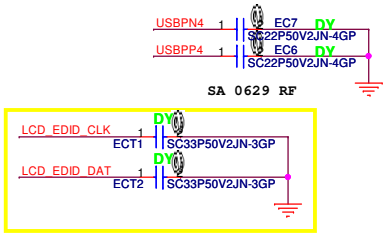
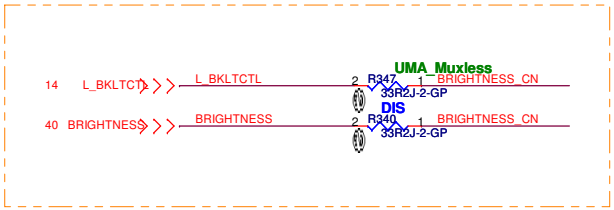
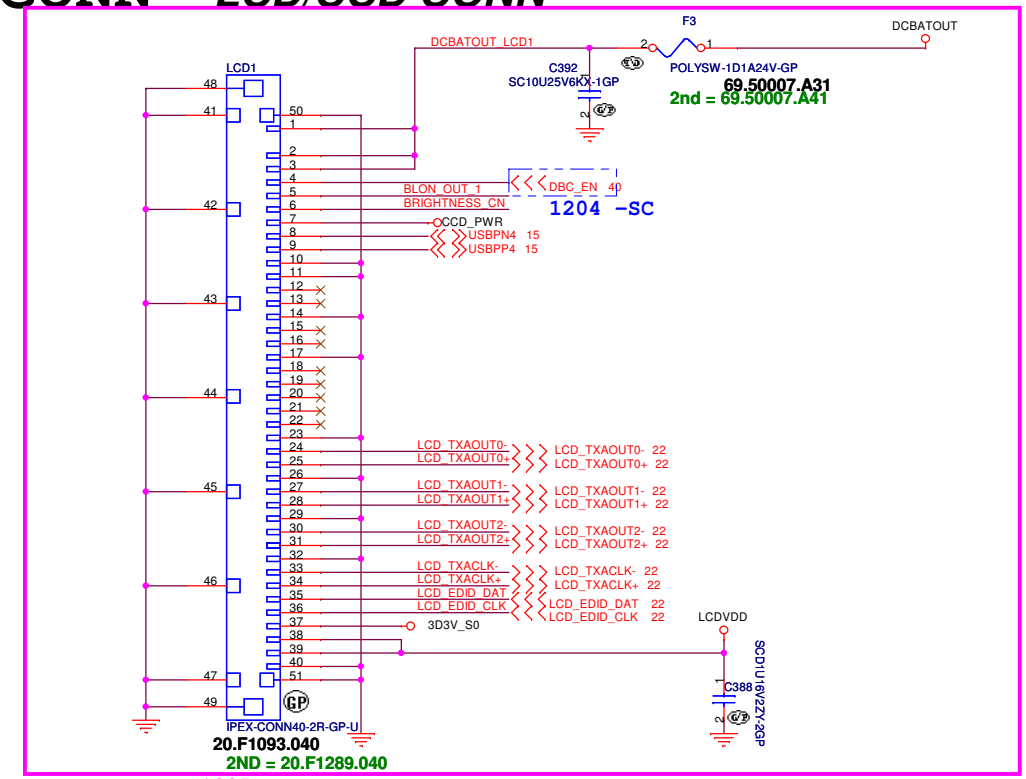
LCD/INVERTER/CCD CONN

LCD/CCD CONN

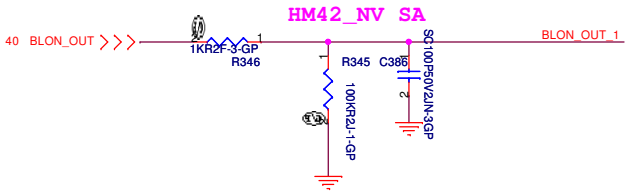


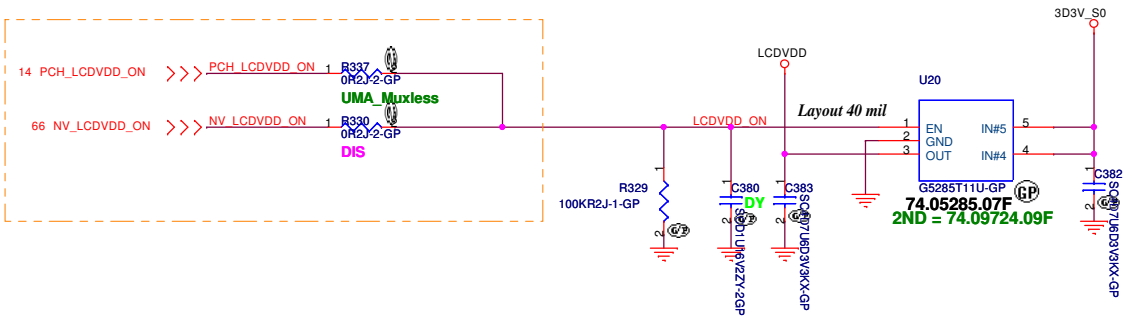




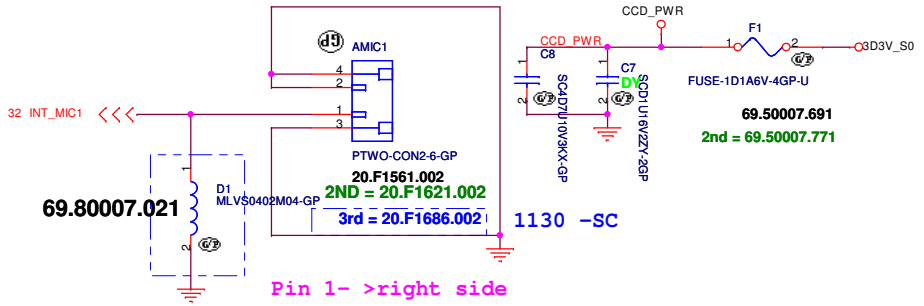
1005 -SA

define same as SJM50-PU,can use SJM50 Cable





Internal Mic



1209 -SC

request by EMI Aaron

Pin 1- >right side

20.F1240.002 Pin1->left side

same as JV70-CP

Diserete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN	
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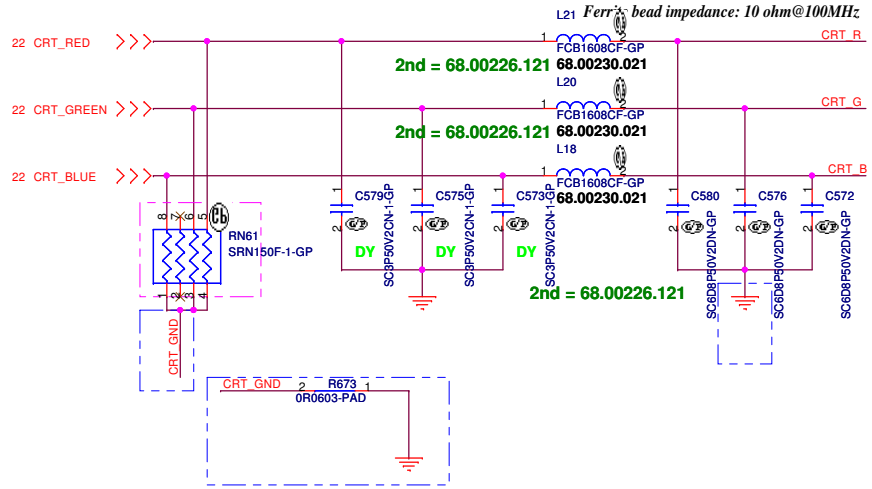
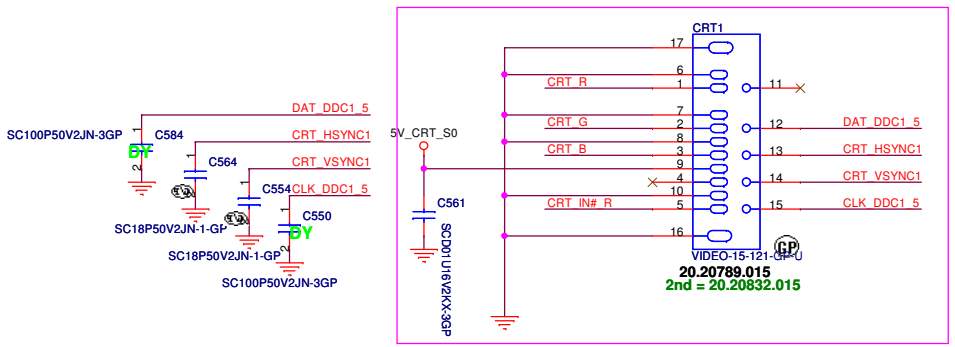
Layout Note:
Place these resistors close to the CRT-out connector

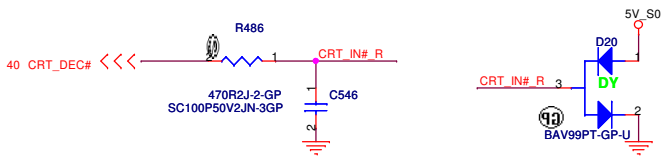


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

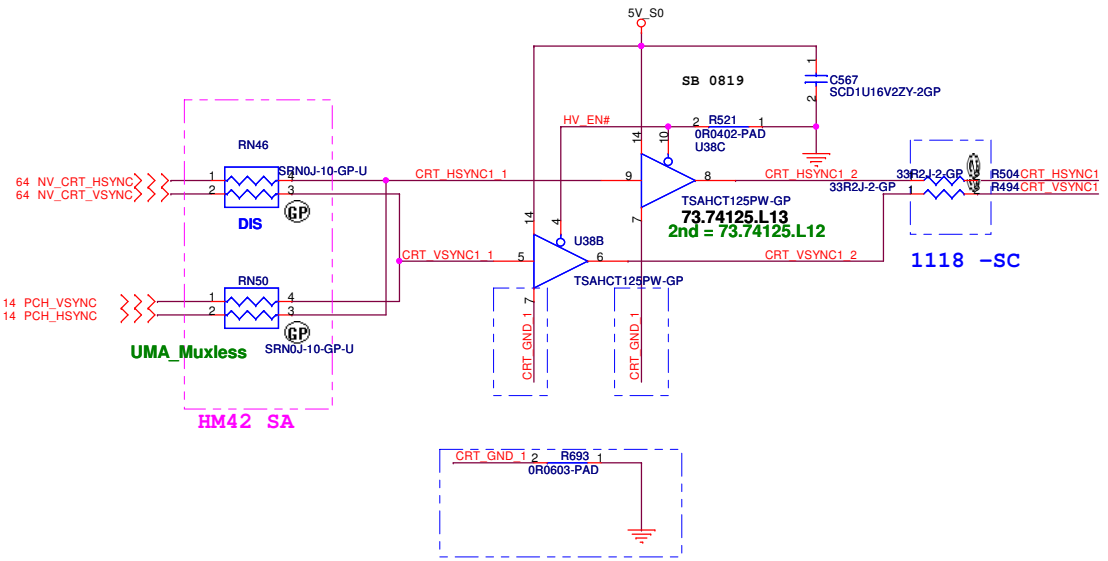


HM42 CP NV Muxless



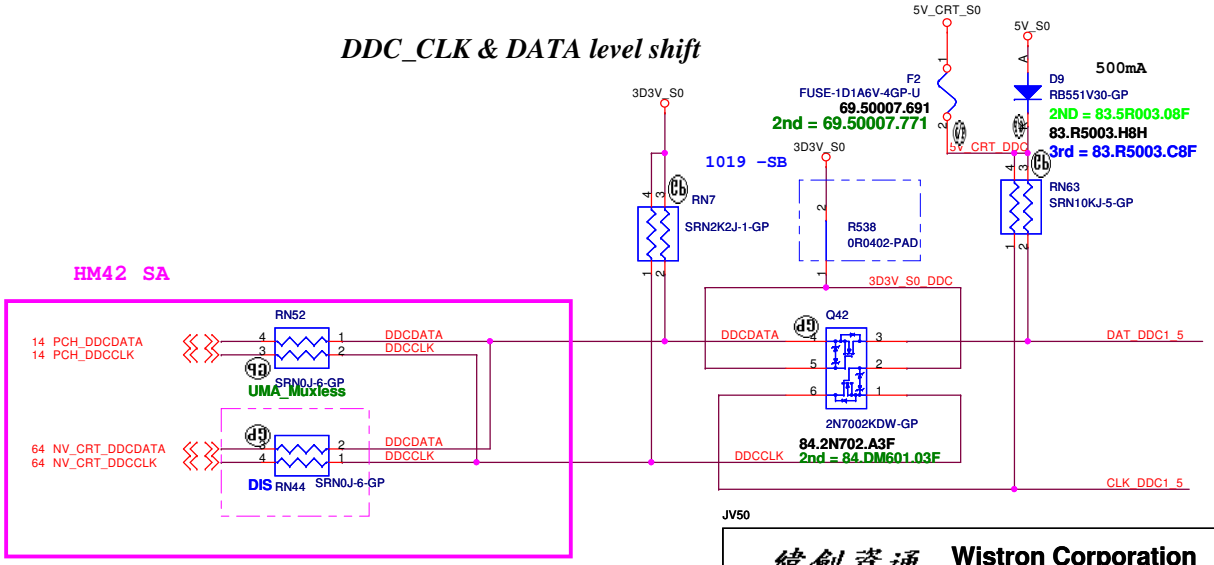
6 1 7 2 8 3 3 9 4 1 0 5

Hsync & Vsync level shift



HM42 SA

DDC_CLK & DATA level shift



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **CRT CONN**		
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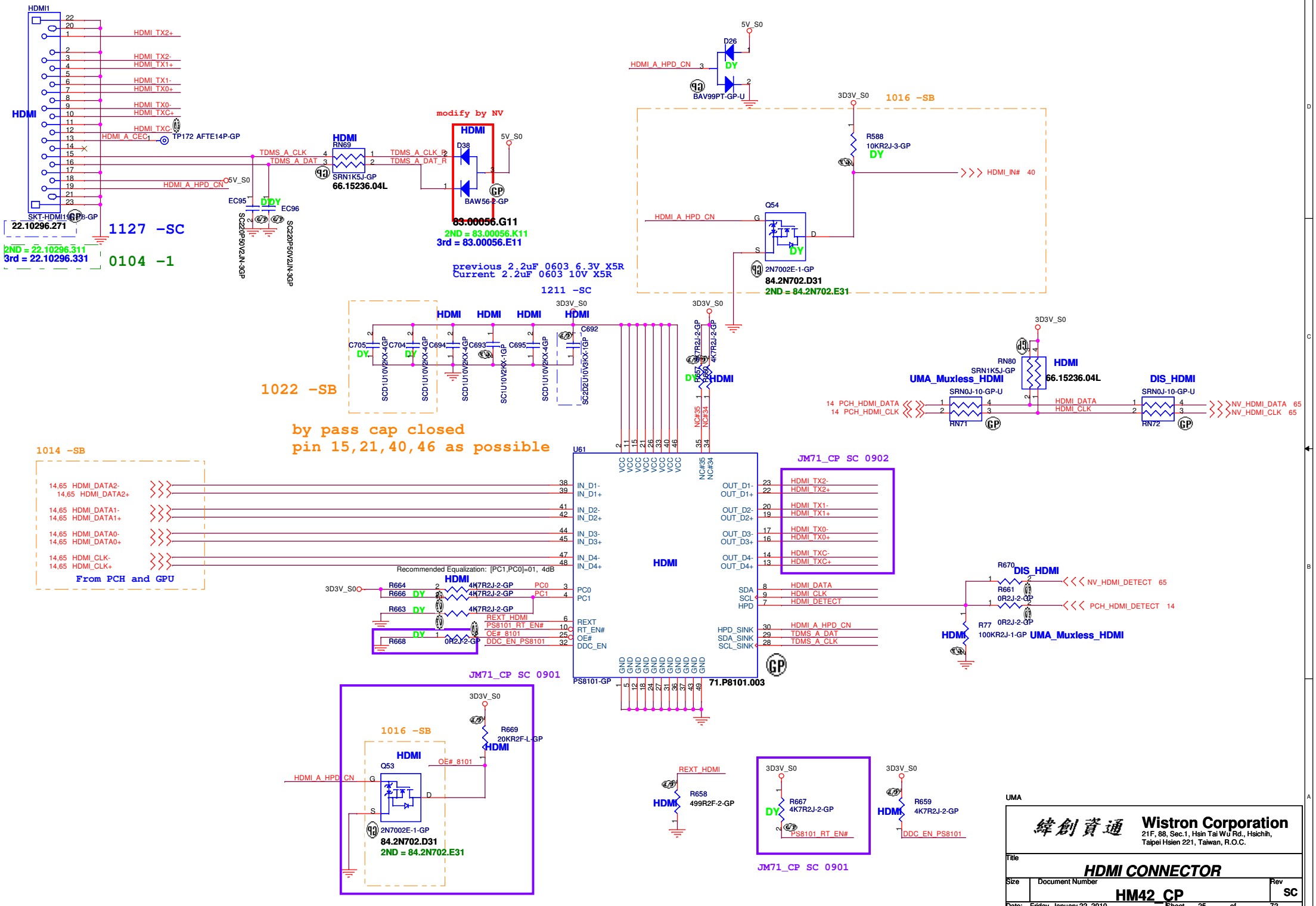

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI CONNECTOR**

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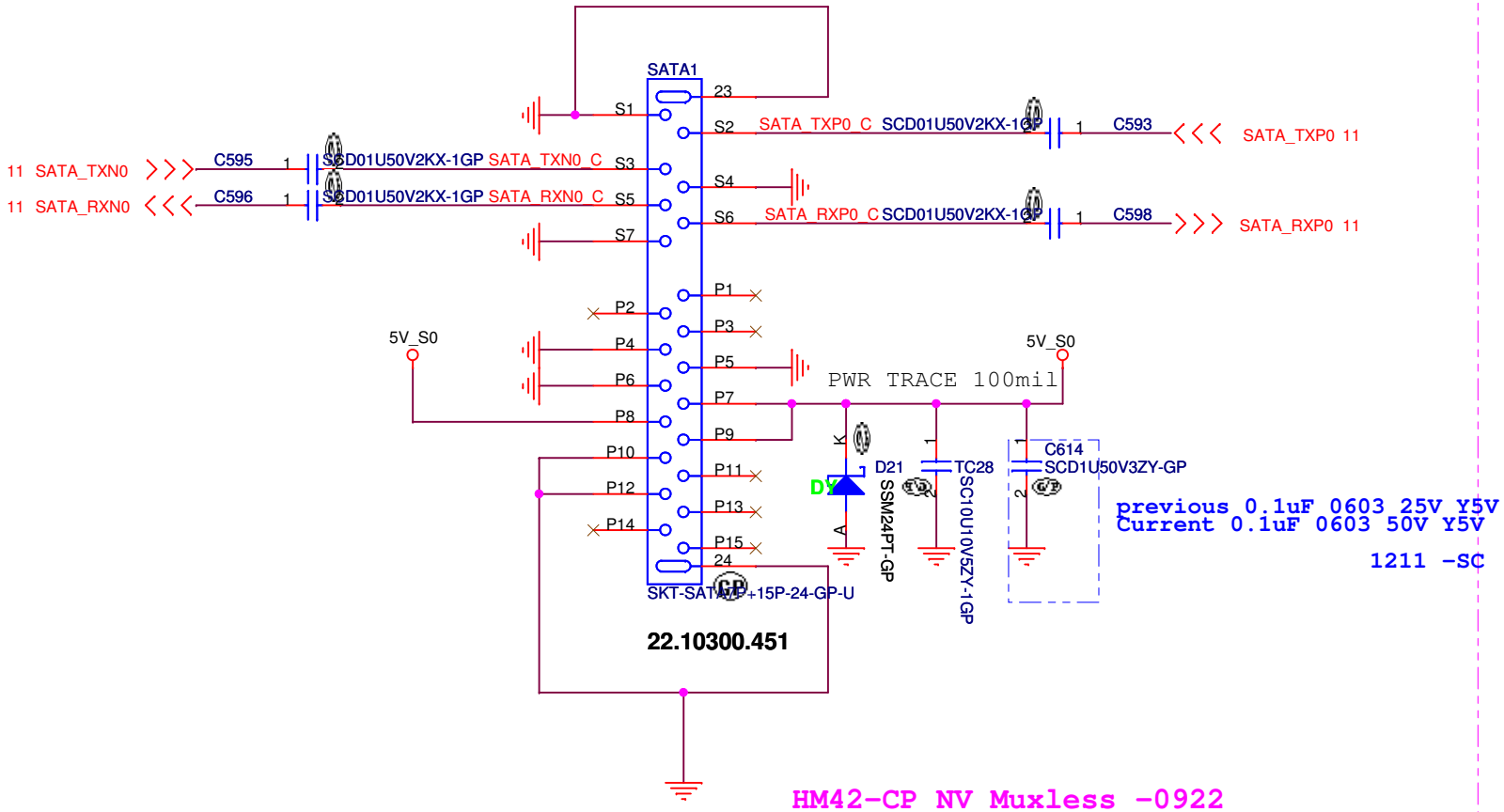
SATA Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
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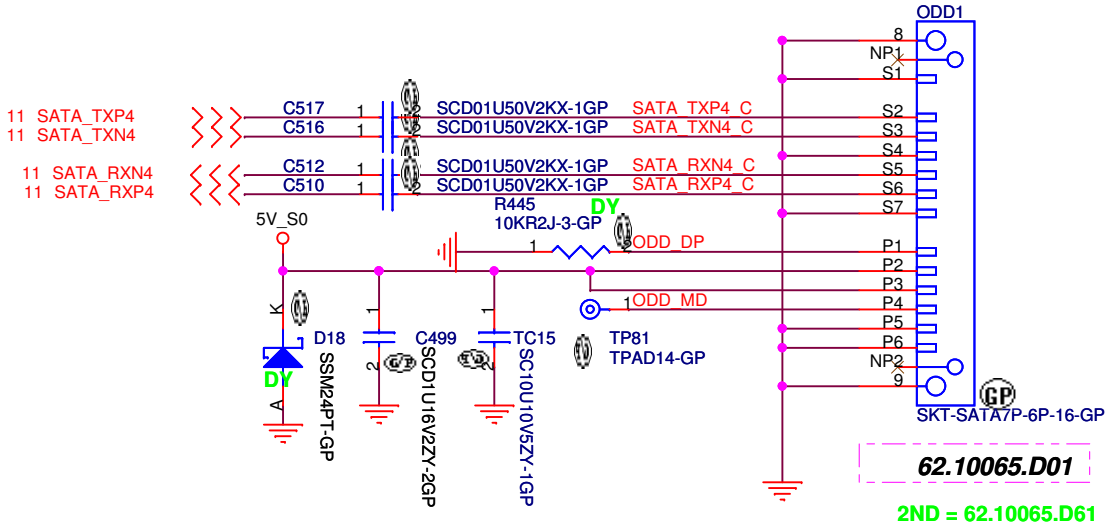
ODD Connector



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***ODD***	
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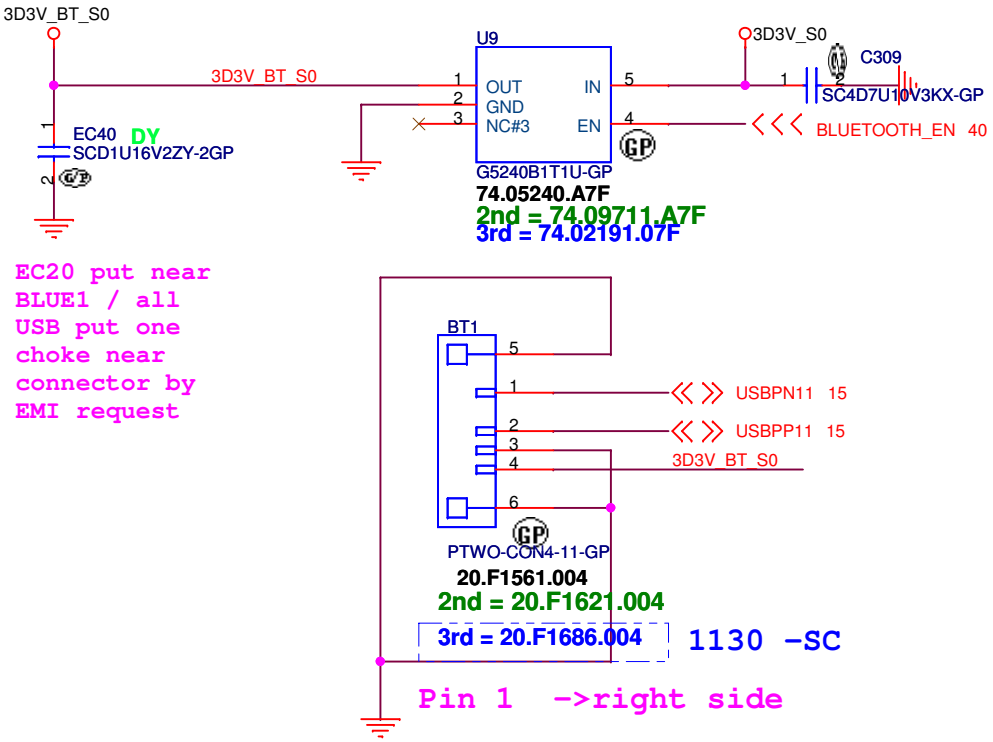
BLUETOOTH MODULE



JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
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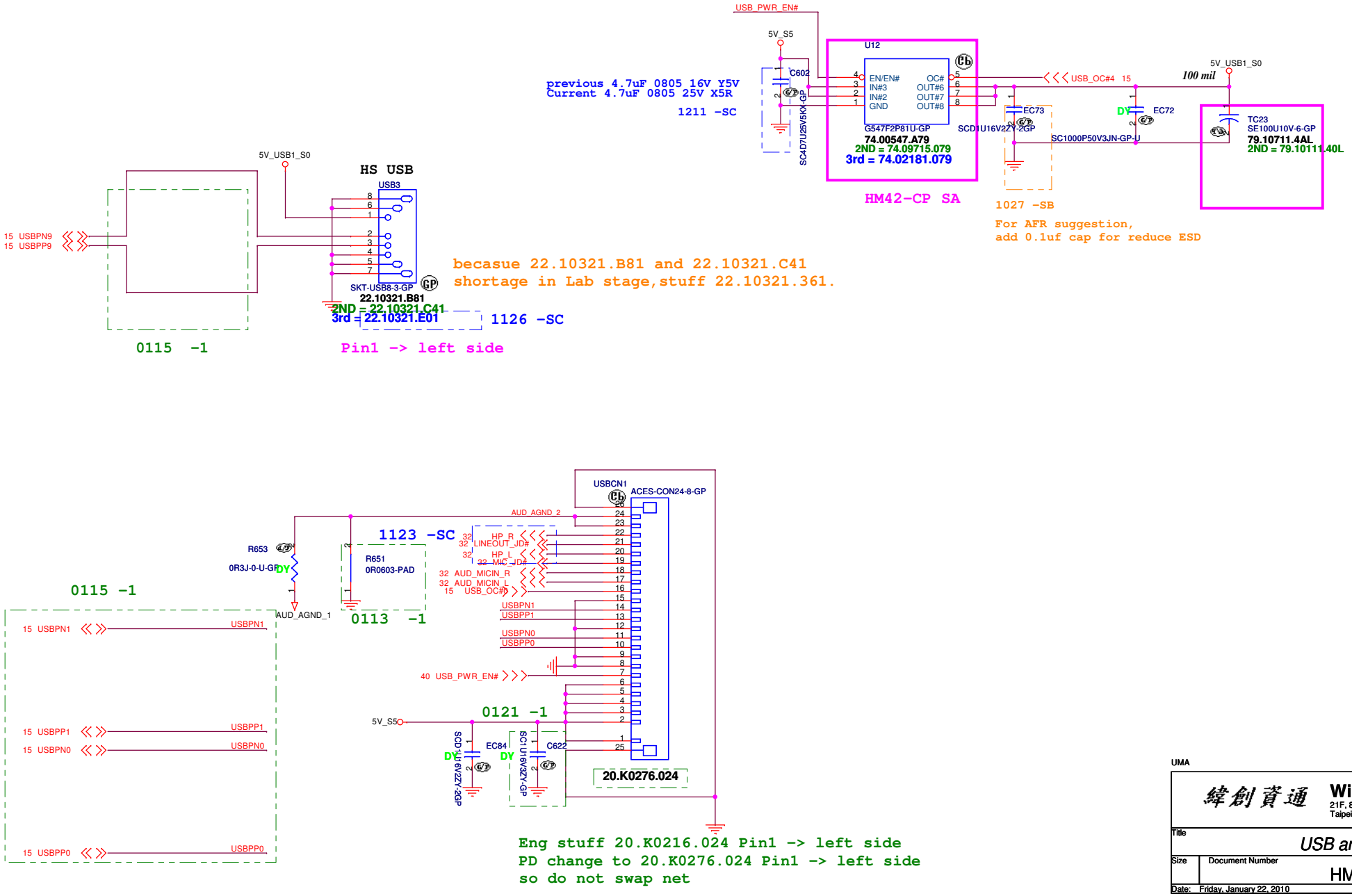

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and Audio CONN

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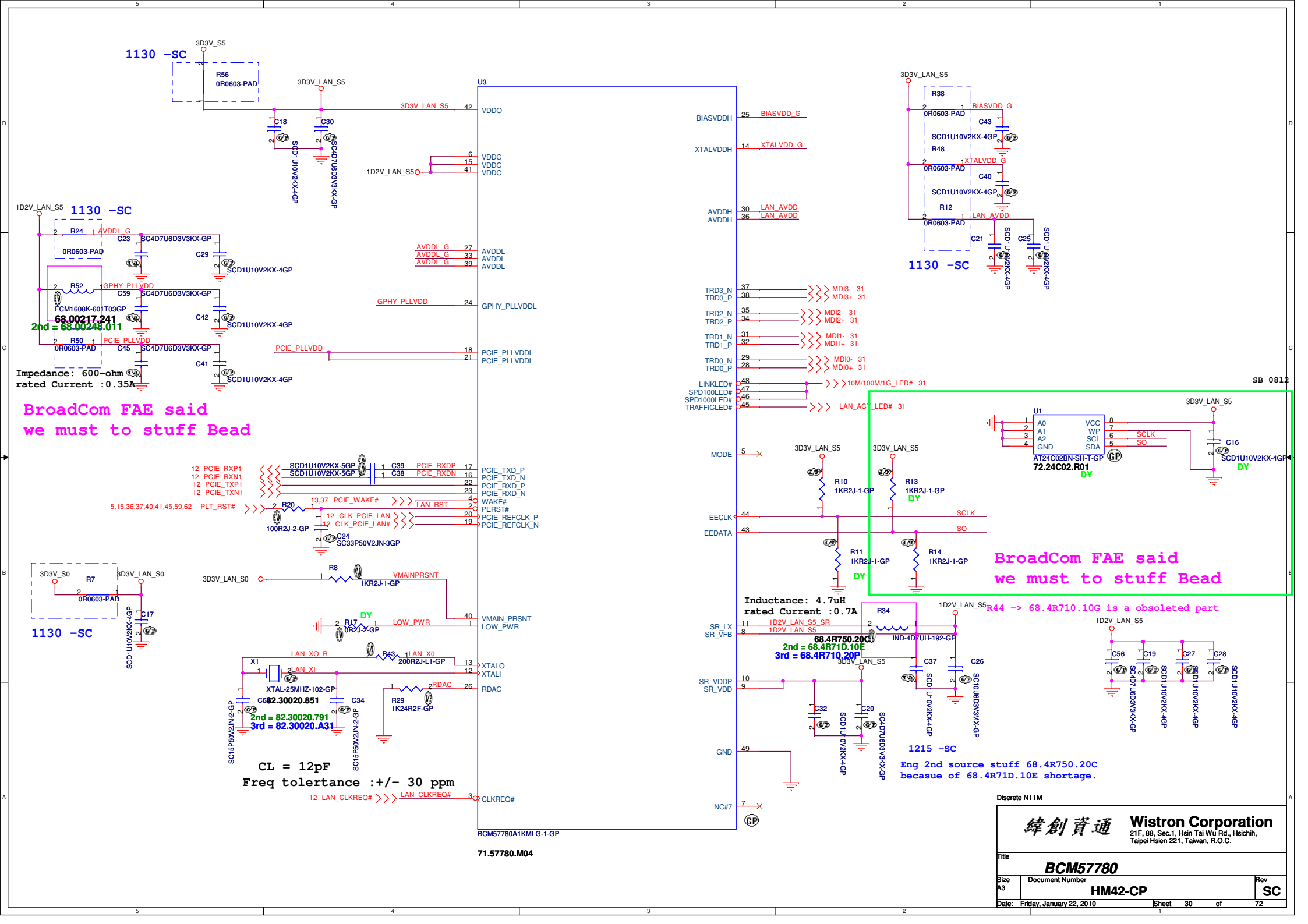
1130 -SC
R56
0R0603-PAD
3D3V_S5
3D3V_LAN_S5
U3
VDDO
VDDC
VDDC
VDDC
1D2V_LAN_S5
C18
C30
SCD1U10V2KX-4GP
SC4D7U6D3V3KX-GP
1130 -SC
R24
0R0603-PAD
AVDDL_G
C23
C29
SC4D7U6D3V3KX-GP
SCD1U10V2KX-4GP
R52
GPHY_PLLVDD
C59
C42
FCM1608K-601T03GP
68.00217.241
2nd = 68.00248.011
R50
PCIE_PLLVDD
C45
C41
Impedance: 600-ohm
rated Current :0.35A
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
BroadCom FAE said
we must to stuff Bead
12 PCIE_RXP1
12 PCIE_RXN1
12 PCIE_TXP1
12 PCIE_TXN1
SCD1U10V2KX-5GP
C39
C38
PCIE_RXDP
PCIE_RXDN
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
5,15,36,37,40,41,45,59,62
PLT_RST#
R20
100R2J-2-GP
13,37 PCIE_WAKE#
LAN_RST
WAKE#
PERST#
12 CLK_PCIE_LAN
12 CLK_PCIE_LAN#
PCIE_REFCLK_P
PCIE_REFCLK_N
C24
SC33P50V2JN-3GP
3D3V_S0
R7
0R0603-PAD
3D3V_LAN_S0
C17
1130 -SC
R8
1KR2J-1-GP
VMAINPRSNT
VMAIN_PRSNT
DY
R17
0R2J-2-GP
LOW_PWR
LOW_PWR
LAN_XO_R
R43
200R2J-L1-GP
LAN_X0
X1
LAN_XI
XTALO
XTALI
XTAL-25MHZ-102-GP
C68
82.30020.851
2nd = 82.30020.791
3rd = 82.30020.A31
C34
SC15P50V2JN-2GP
R29
1K24R2F-GP
RDAC
RDAC
CL = 12pF
Freq tolertance :+/- 30 ppm
12 LAN_CLKREQ#
LAN_CLKREQ#
CLKREQ#
BCM57780A1KMLG-1-GP
71.57780.M04
BIASVDDH
XTALVDDH
AVDDH
AVDDH
BIASVDD_G
XTALVDD_G
LAN_AVDD
LAN_AVDD
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
MDI3- 31
MDI3+ 31
MDI2- 31
MDI2+ 31
MDI1- 31
MDI1+ 31
MDI0- 31
MDI0+ 31
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
10M/100M/1G_LED# 31
LAN_ACT_LED# 31
MODE
EECLK
EEDATA
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND
NC#7
3D3V_LAN_S5
R38
0R0603-PAD
C43
SCD1U10V2KX-4GP
R48
C40
R12
C21
C25
1130 -SC
SB 0812
U1
AT24C02BN-SH-T-GP
72.24C02.R01
DY
SCLK
SO
C16
R10
1KR2J-1-GP
R13
1KR2J-1-GP
R11
1KR2J-1-GP
R14
1KR2J-1-GP
BroadCom FAE said
we must to stuff Bead
Inductance: 4.7uH
rated Current :0.7A
R34
1D2V_LAN_S5_SR
1D2V_LAN_S5
68.4R750.20C
2nd = 68.4R71D.10E
3rd = 68.4R710.20P
IND-4D7UH-192-GP
R44 -> 68.4R710.10G is a obsoleted part
C37
C26
C32
C20
1215 -SC
Eng 2nd source stuff 68.4R750.20C
becasue of 68.4R71D.10E shortage.
C56
C19
C27
C28
Diserete N11M
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size
A3
Document Number
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SC
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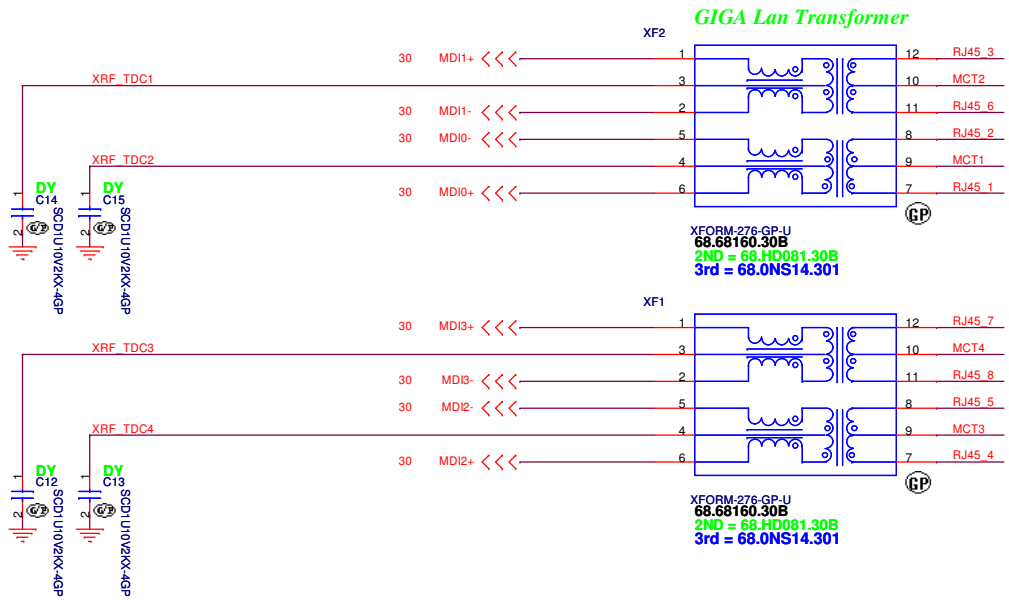
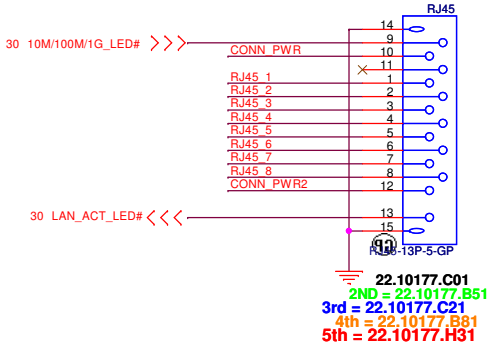
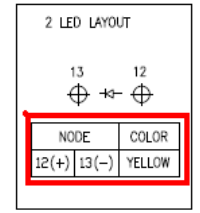
LAN Connector

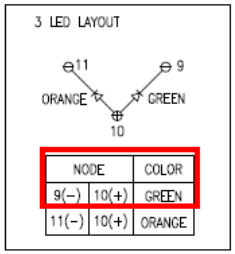
LAN Connector

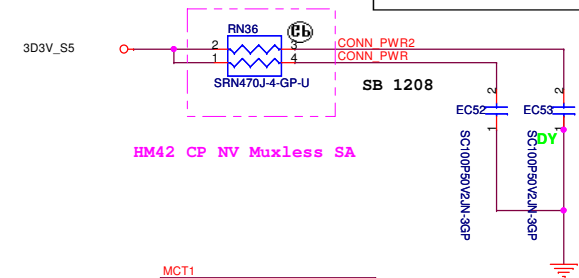
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

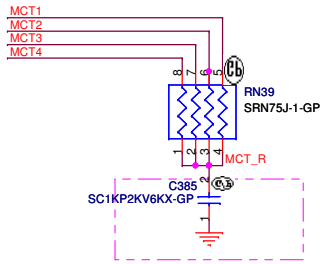


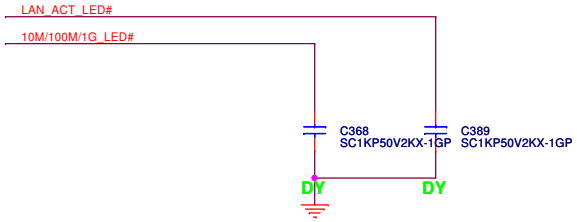












UMA

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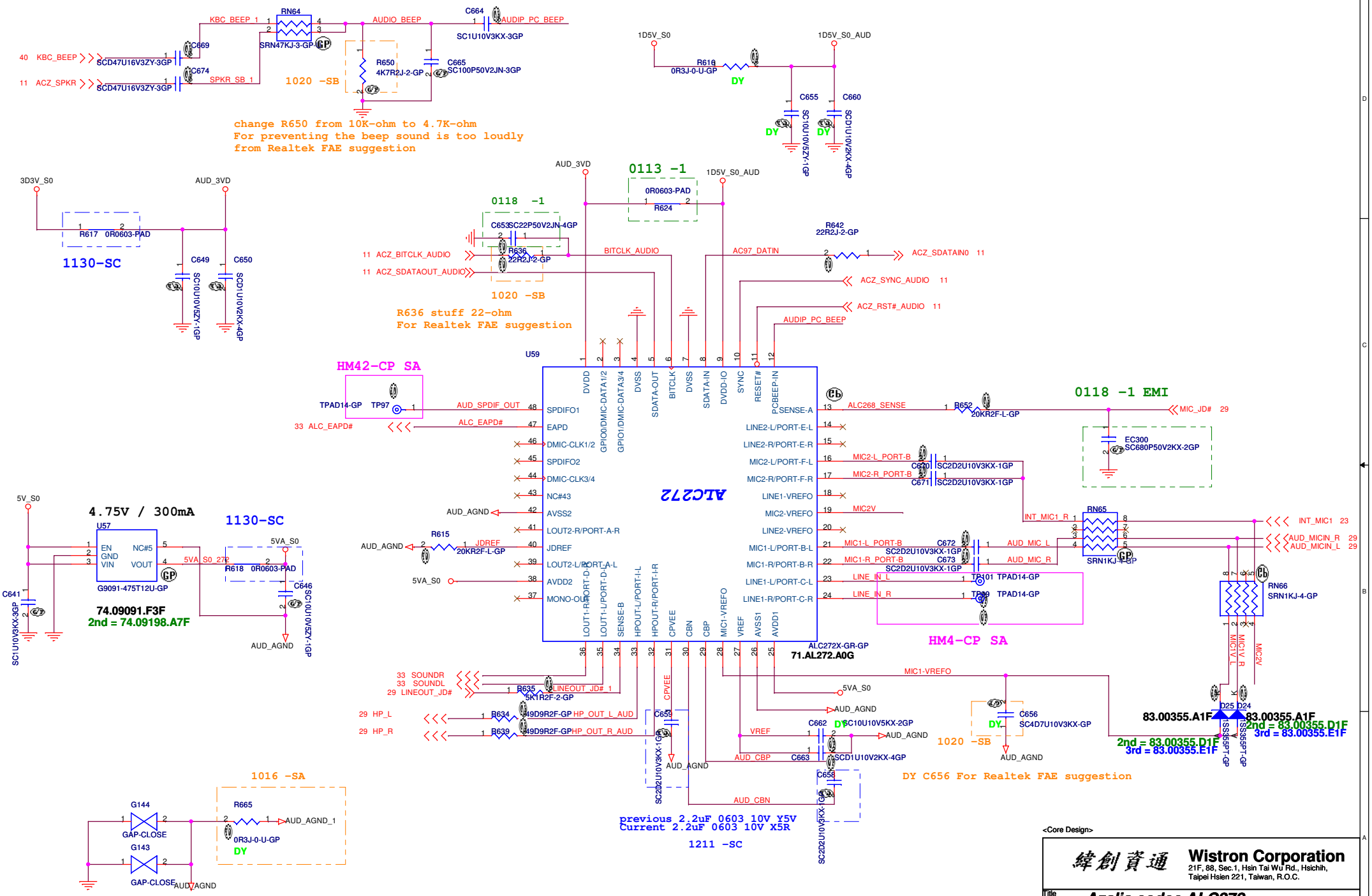
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN CONN		
Size: A3	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 31 of 72	



<Core Design>

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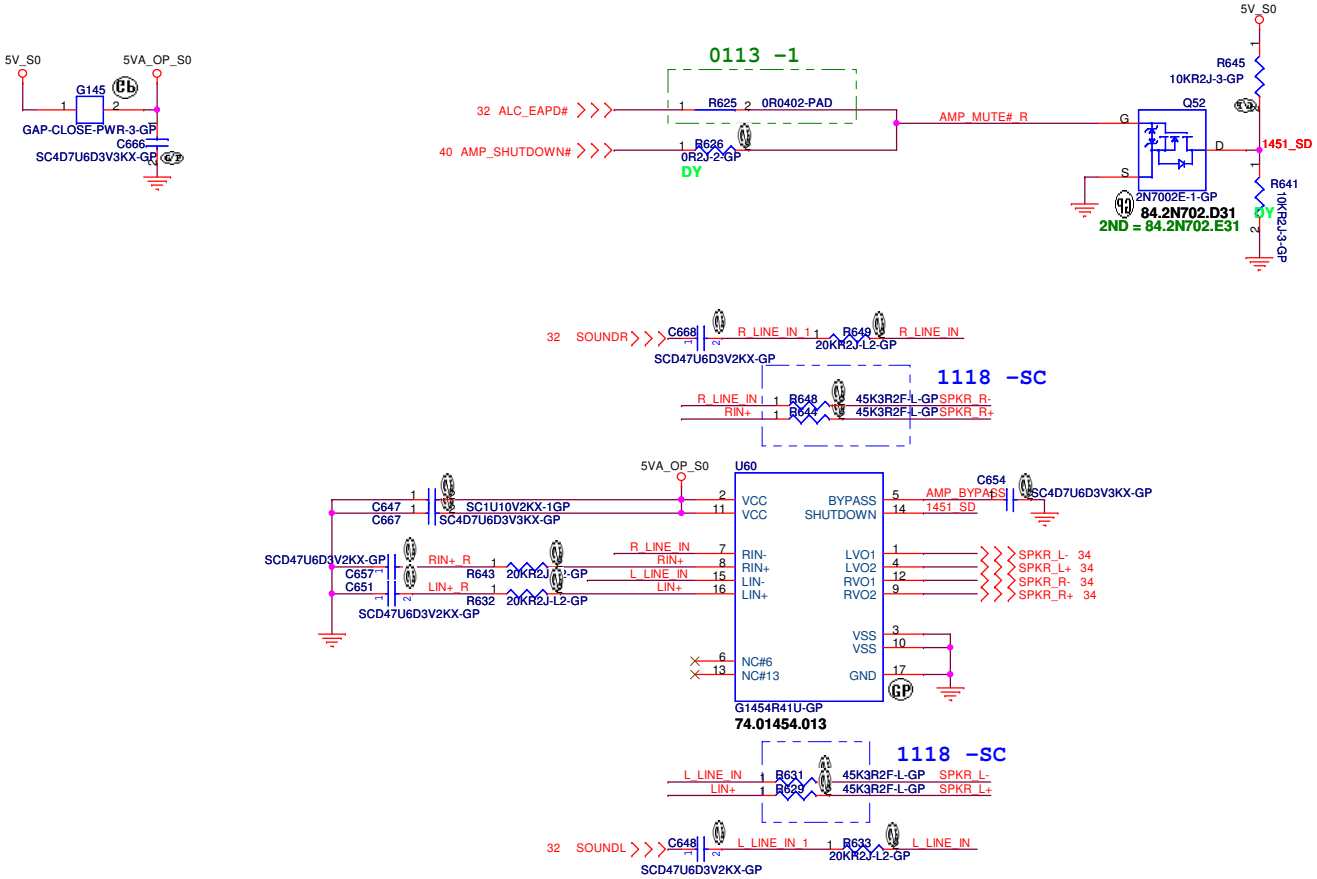
Title: Azalia codec ALC272

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 32 of 72



Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.446^2/4=1.5W

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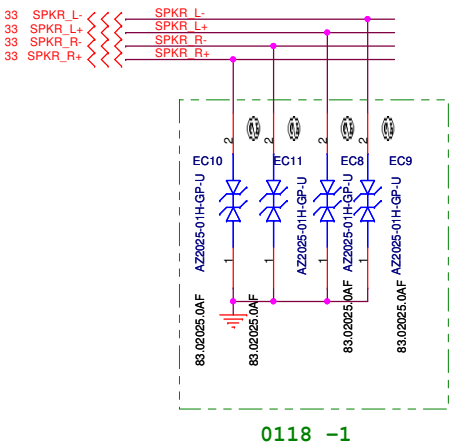
Taipei Hsien 221, Taiwan, R.O.C.

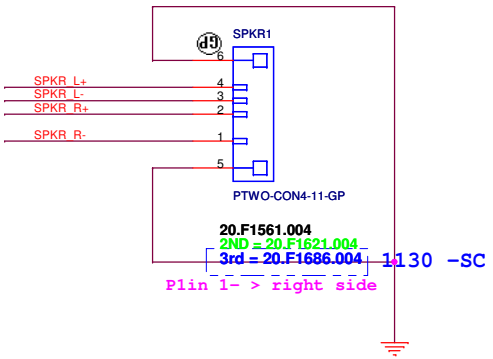
Title: AUDIO AMP

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 33 of 72

Internal Speaker





Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO SPEARK*		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 34 of 72	

JV50

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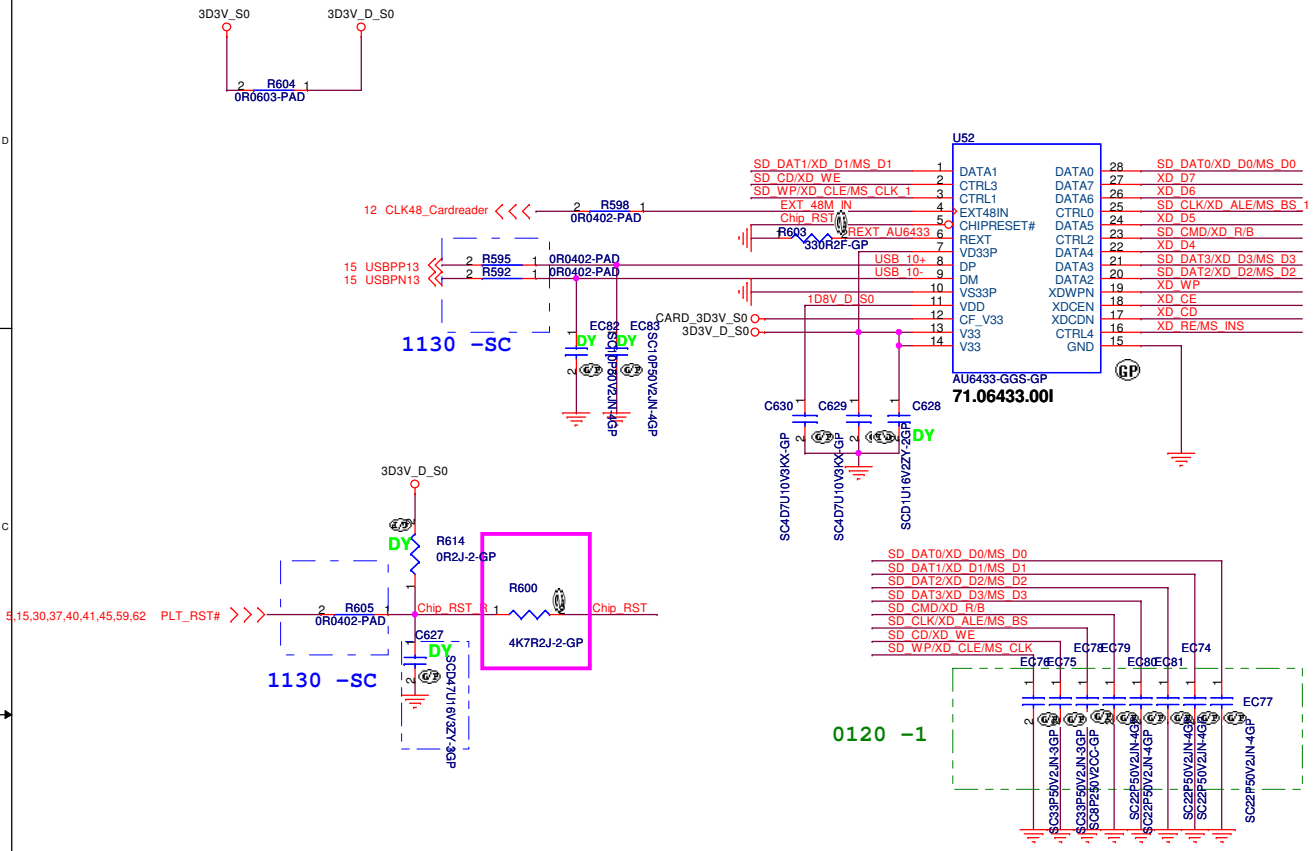
Taipei Hsien 221, Taiwan, R.O.C.

Title
Resrve_MDC

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 35 of 72

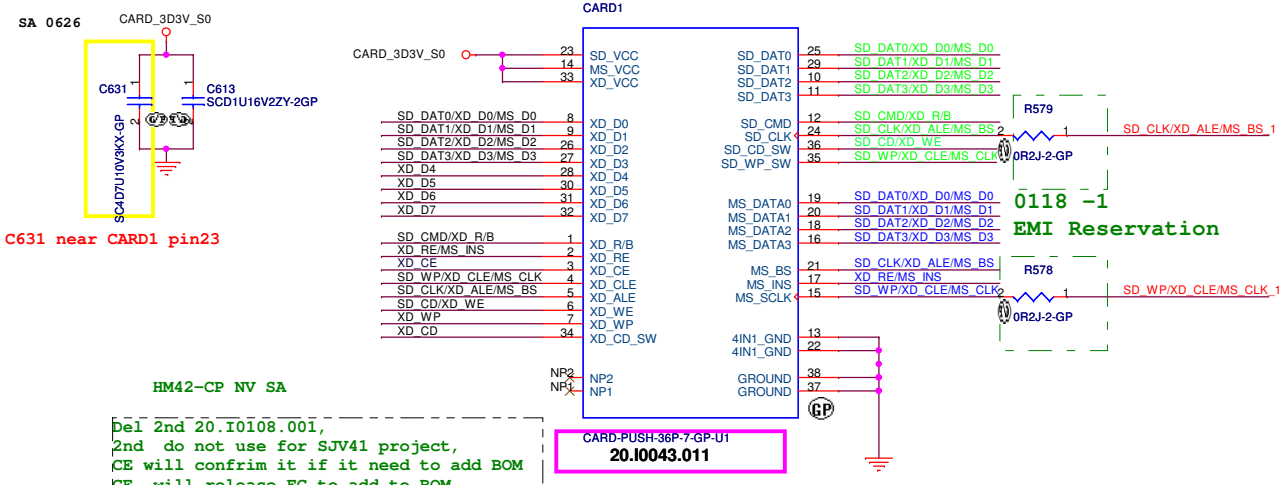


Pin	SD Mode	
	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]
2	CMD	Command/Response
3	VSS1	Supply voltage ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]
8	DAT1	Data line[Bit 1]
9	DAT2	Data line[Bit 2]

Pin No.	SD/MMC	MS/MS PRO	xD
P1 xD-R/B			2P
P2 xD-RE			3P
P3 xD-CE			4P
P4 xD-CLE			5P
P5 xD-ALE			6P
P6 xD-WE			7P
P7 xD-WP			8P
P8 xD-D0			10P
P9 xD-D1			11P
P10 SD-DAT2	9P		
P11 SD-DAT3	1P		
P12 SD-CMD	2P		
P13 4in1-GND	3P/6P	1P/10P	1P/9P
P14 MS-VCC		9P	
P15 MS-SCLK		8P	
P16 MS-DATA3		7P	
P17 MS-INS		6P	
P18 MS-DATA2		5P	
P19 MS-DATA0		4P	

Pin No.	SD/MMC	MS/MS PRO	xD
P20 MS-DATA1		3P	
P21 MS-BS		2P	
P22 4in1-GND	3P/6P	1P/10P	1P/9P
P23 SD-VCC	4P		
P24 SD-CLK	5P		
P25 SD-DAT0	7P		
P26 xD-D2			12P
P27 xD-D3			13P
P28 xD-D4			14P
P29 SD-DAT1	8P		
P30 xD-D5			15P
P31 xD-D6			16P
P32 xD-D7			17P
P33 xD-VCC			18P
P34 XD-CD-SW			19P
P35 SD-WP-SW	SD-WP-SW		
P36 SD-CD-SW	SD-CD-SW		
P37 P38	4 IN 1-GND	SD-WP/CD-SW-GND	

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



HM42-CP NV SA

Del 2nd 20.I0108.001,
2nd do not use for SJV41 project,
CE will confrim it if it need to add BOM
CE will release EC to add to BOM

Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2,7V - 3,6V)
10	VSS	Vss

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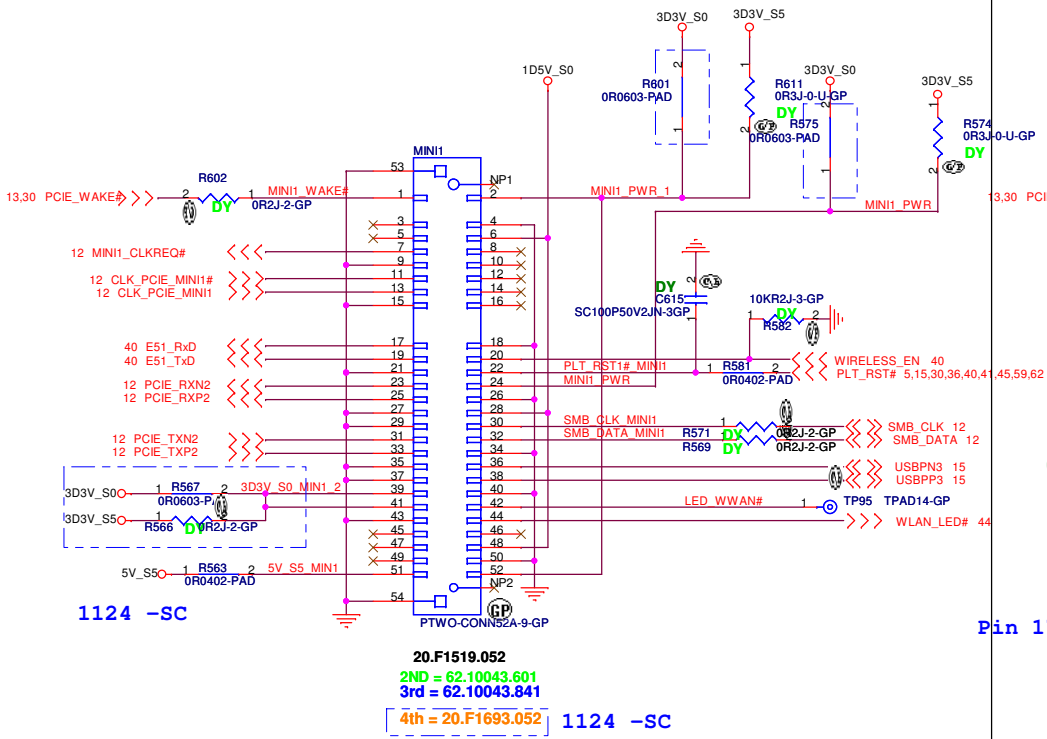
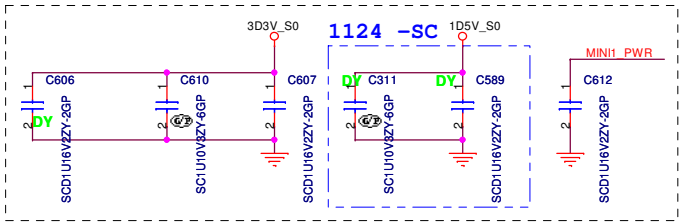
Title: Cardreader
Size | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 | Sheet 36 of 72

Mini Card Connector(WLAN)
Support debug-card

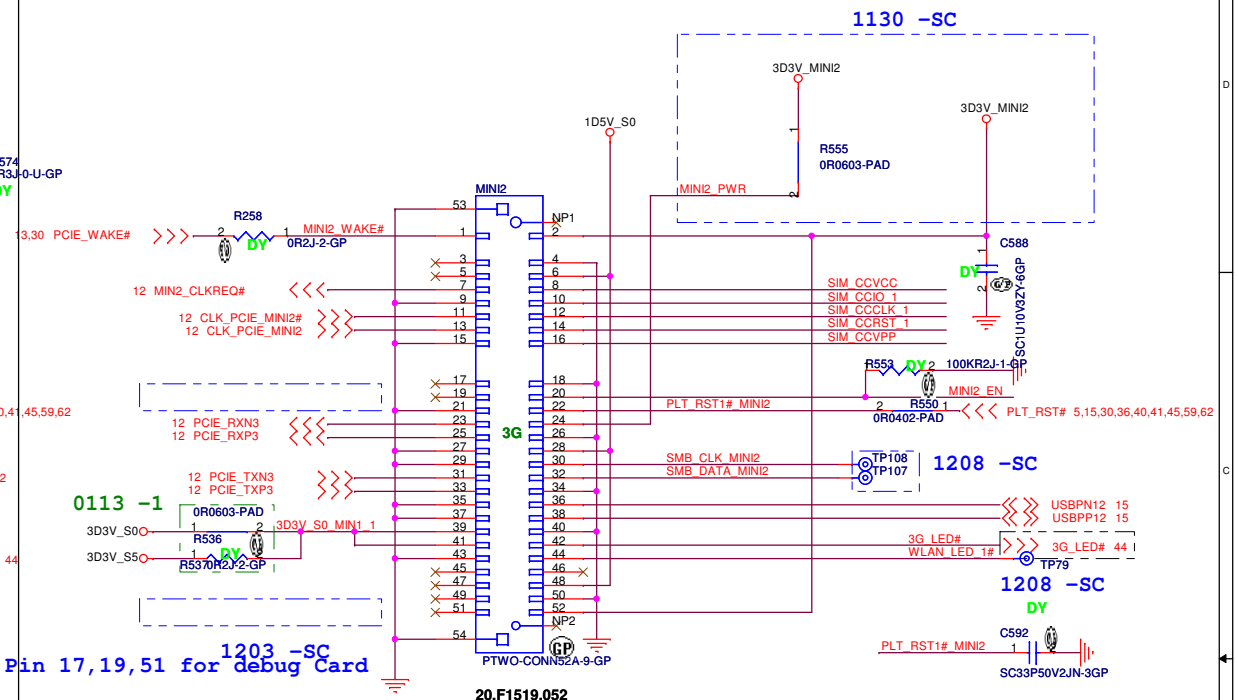


20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC

Place near MINI1

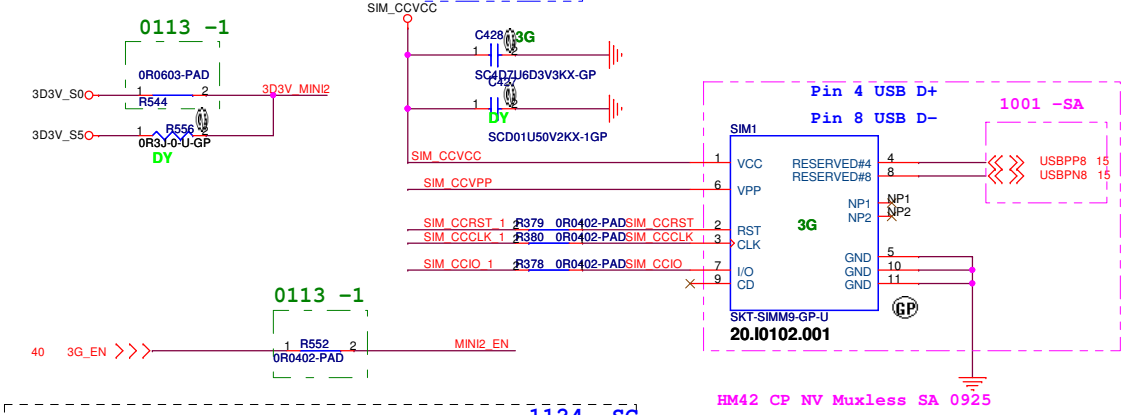


Mini Card Connector(Robson2 and 3G)

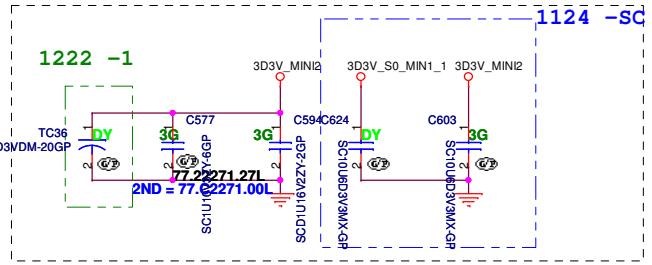


Pin 17,19,51 for debug Card

20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC



HM42 CP NV Muxless SA 0925



Diserete N11M

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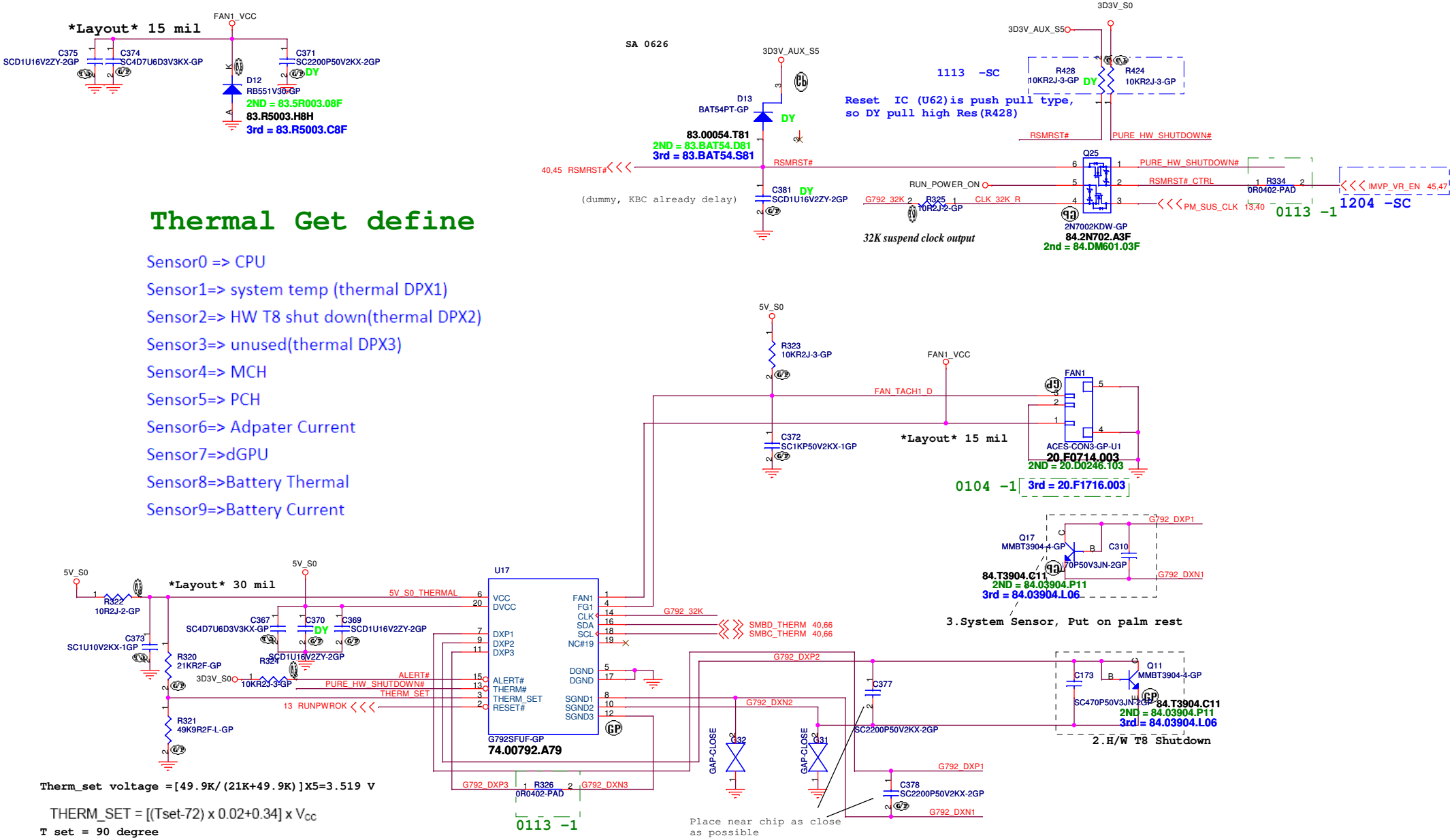
Title: MINI CARD		
Size: A3	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 37 of 72	



UMA

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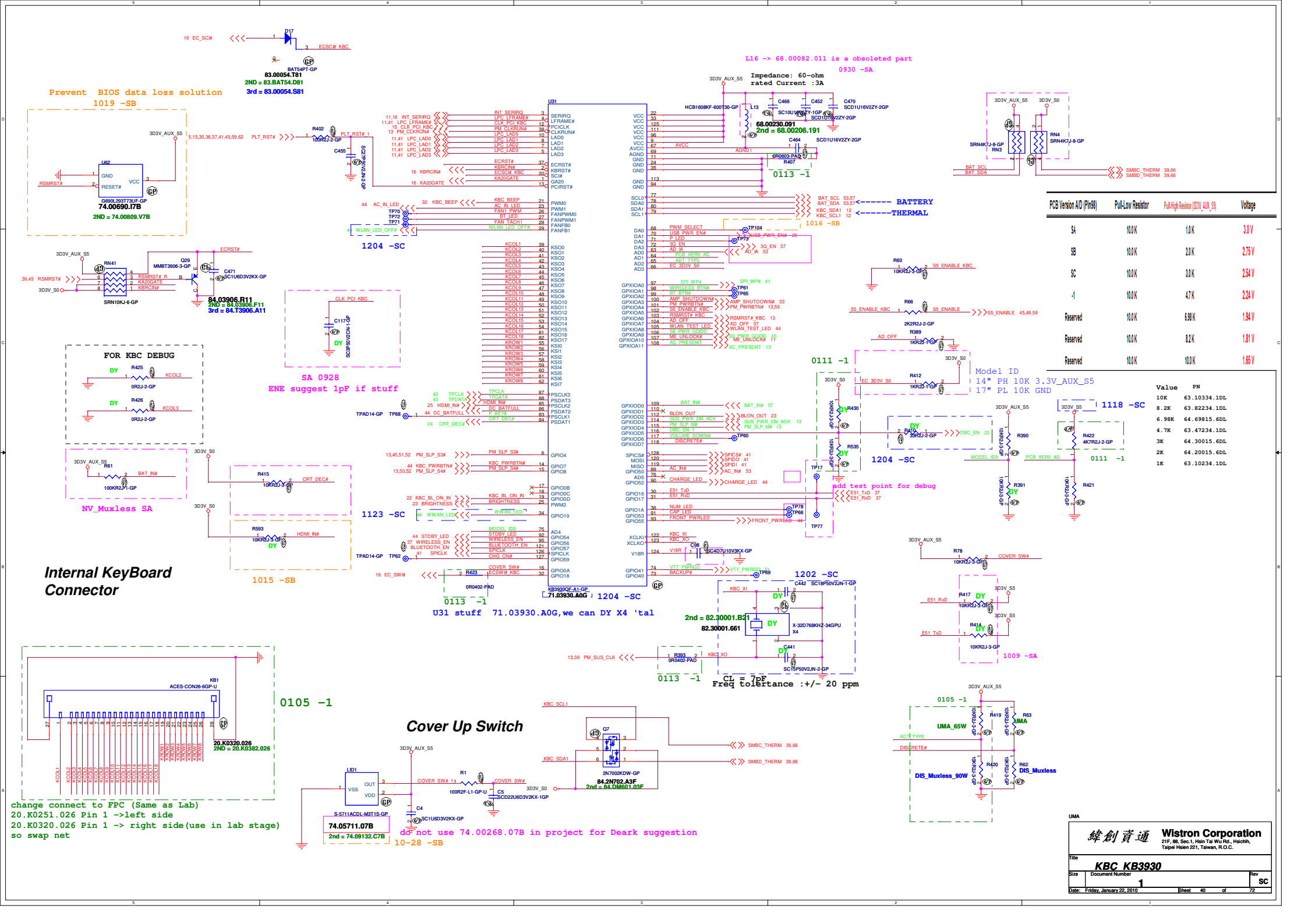
Title: ***Thermal/Fan Connector***

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 39 of 72



PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	10.0 K	1.0 K	3.0 V
SB	10.0 K	2.0 K	2.75 V
SC	10.0 K	3.0 K	2.54 V
-1	10.0 K	4.7 K	2.24 V
Reserved	10.0 K	6.98 K	1.94 V
Reserved	10.0 K	8.2 K	1.81 V
Reserved	10.0 K	10.0 K	1.65 V

Value	PN
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL

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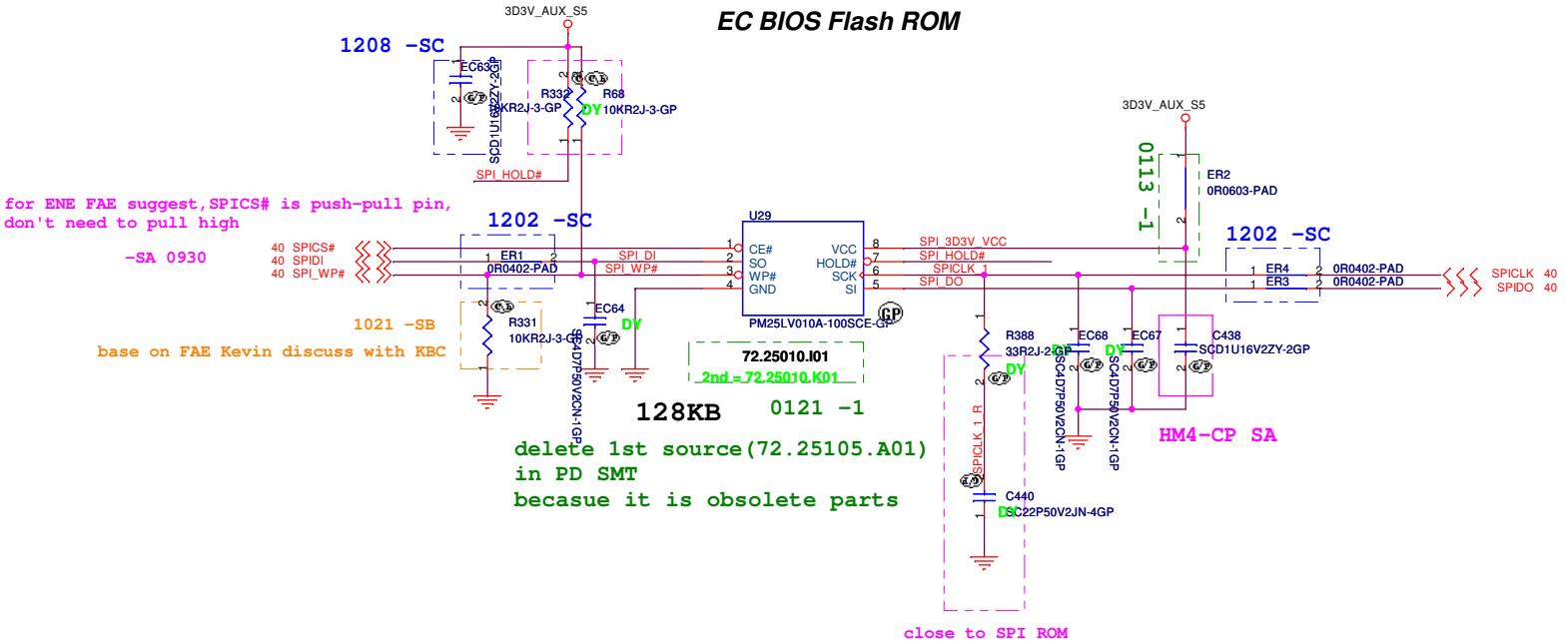
Title: KBC_KB3930

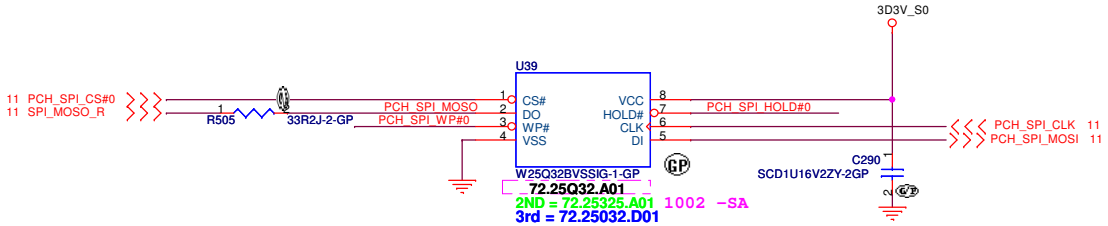
Size	Document Number	Rev
	1	SC

Date: Friday, January 22, 2010 Sheet 40 of 72

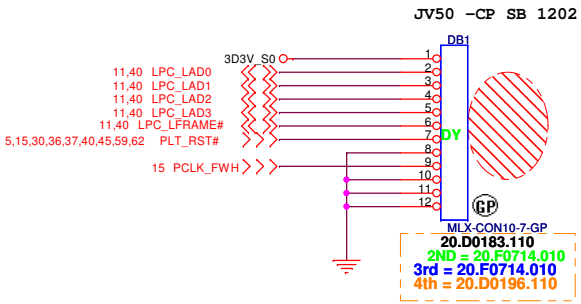
EC BIOS Flash ROM

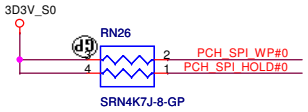


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





Diserete N11M

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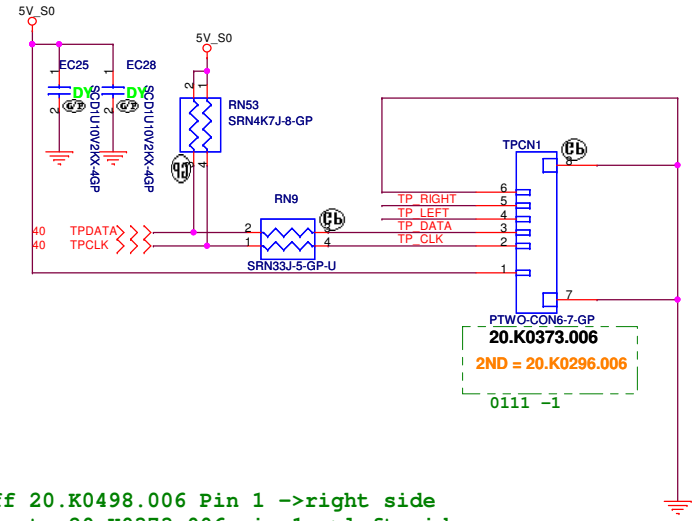
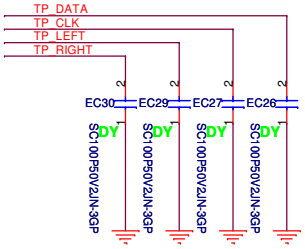
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

Size	Document Number	Rev
	HM42-CP	SC

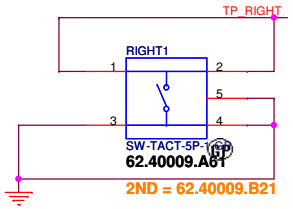
Date: Friday, January 22, 2010 Sheet 41 of 72



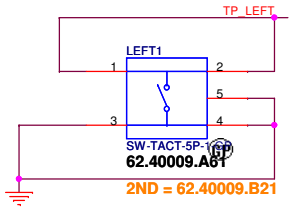


Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically

RIGHT



LEFT



Diserete N11M

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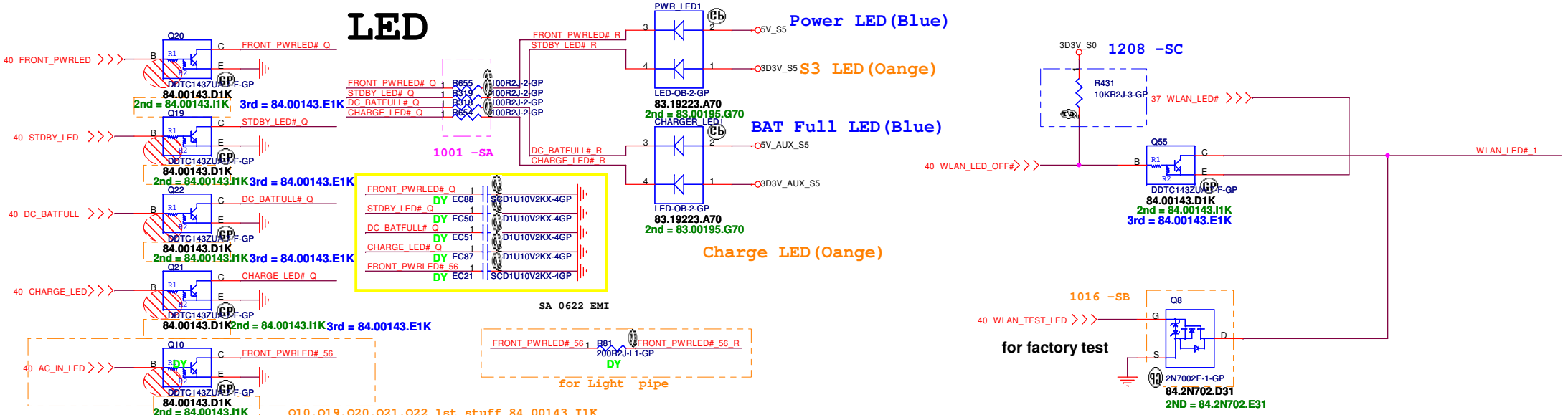
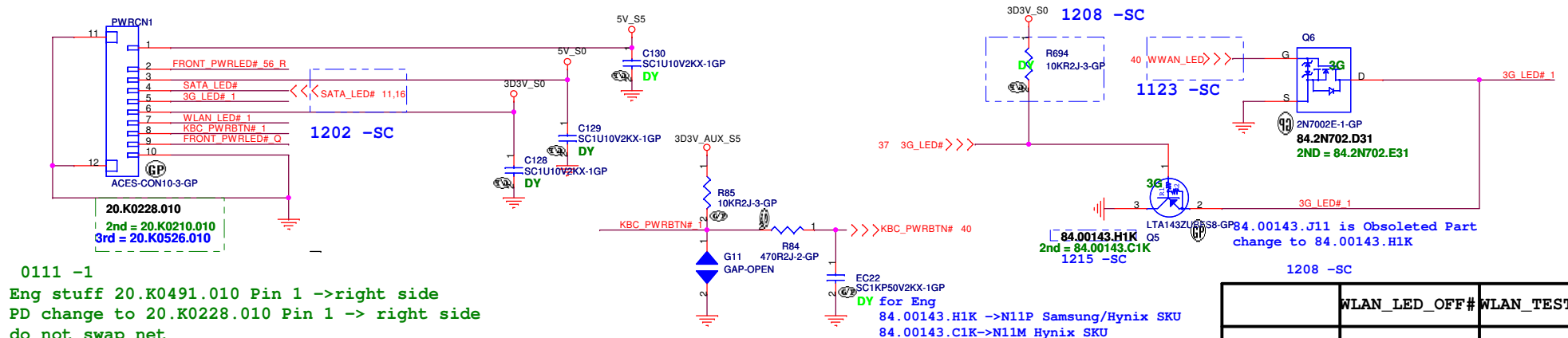
Title: *Touch PAD*		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 43 of 72	

LED



For 2010 Acer Project, WLAN and 3G LED control by KBC



0111 -1
Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net

84.00143.H1K ->N11P Samsung/Hynix SKU
84.00143.C1K->N11M Hynix SKU

Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED&POWERBD CONN

Size | Document Number: HM42-CP | Rev: SC

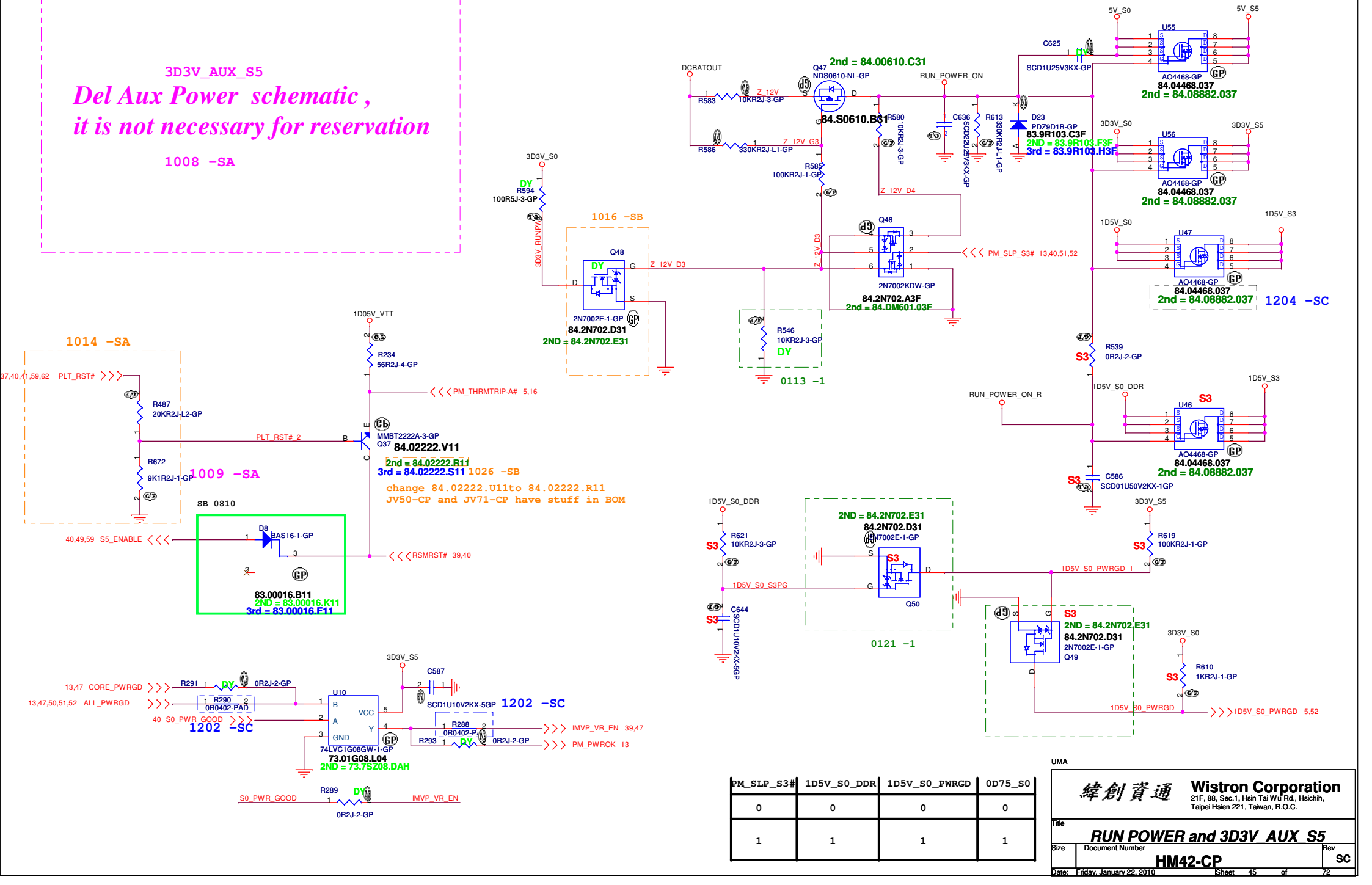
Date: Friday, January 22, 2010 | Sheet 44 of 72

Run Power

3D3V_AUX_S5

Del Aux Power schematic ,
it is not necessary for reservation

1008 -SA



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

UMA

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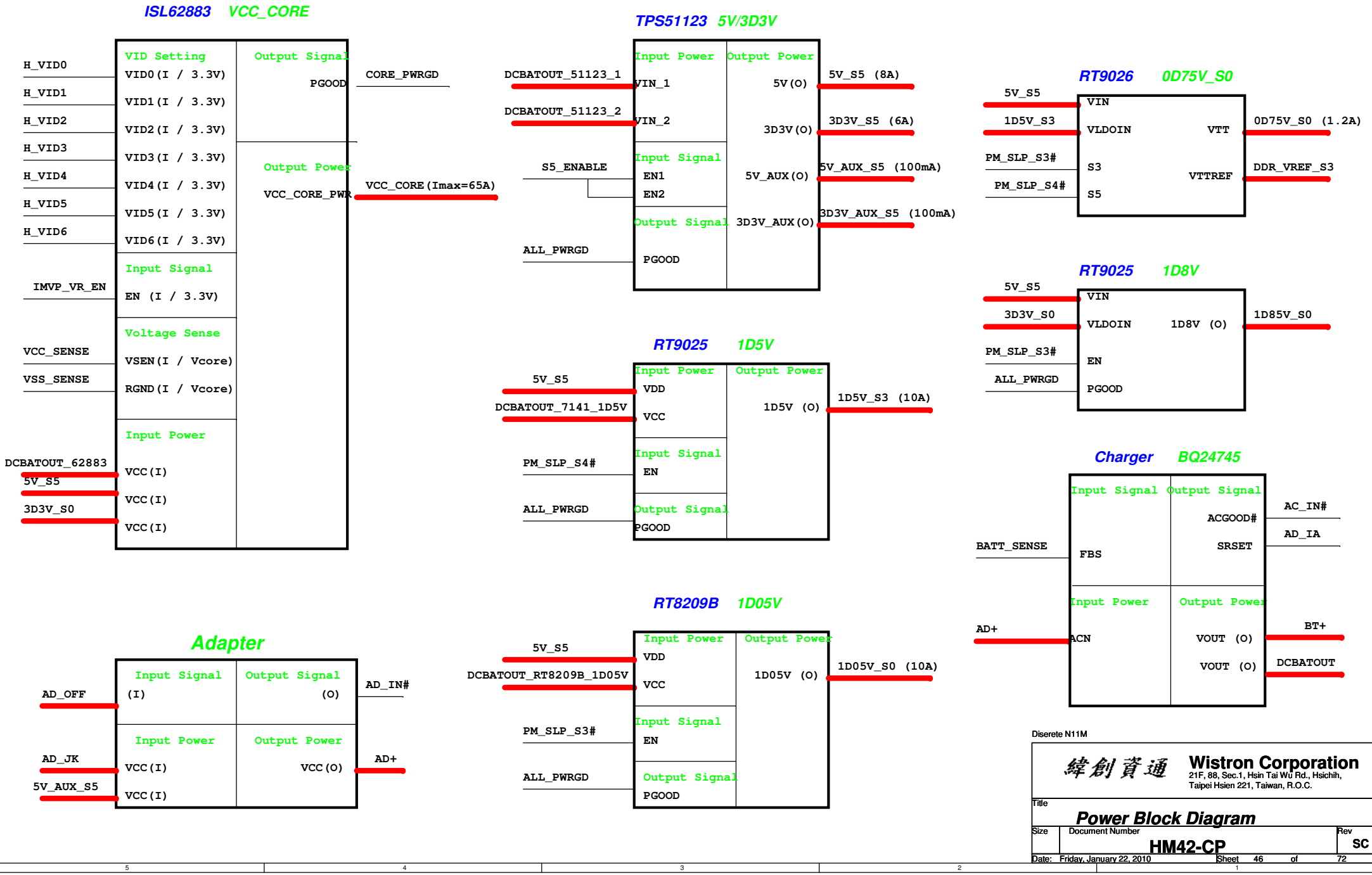
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V_AUX_S5**

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 45 of 72



Diserete N11M

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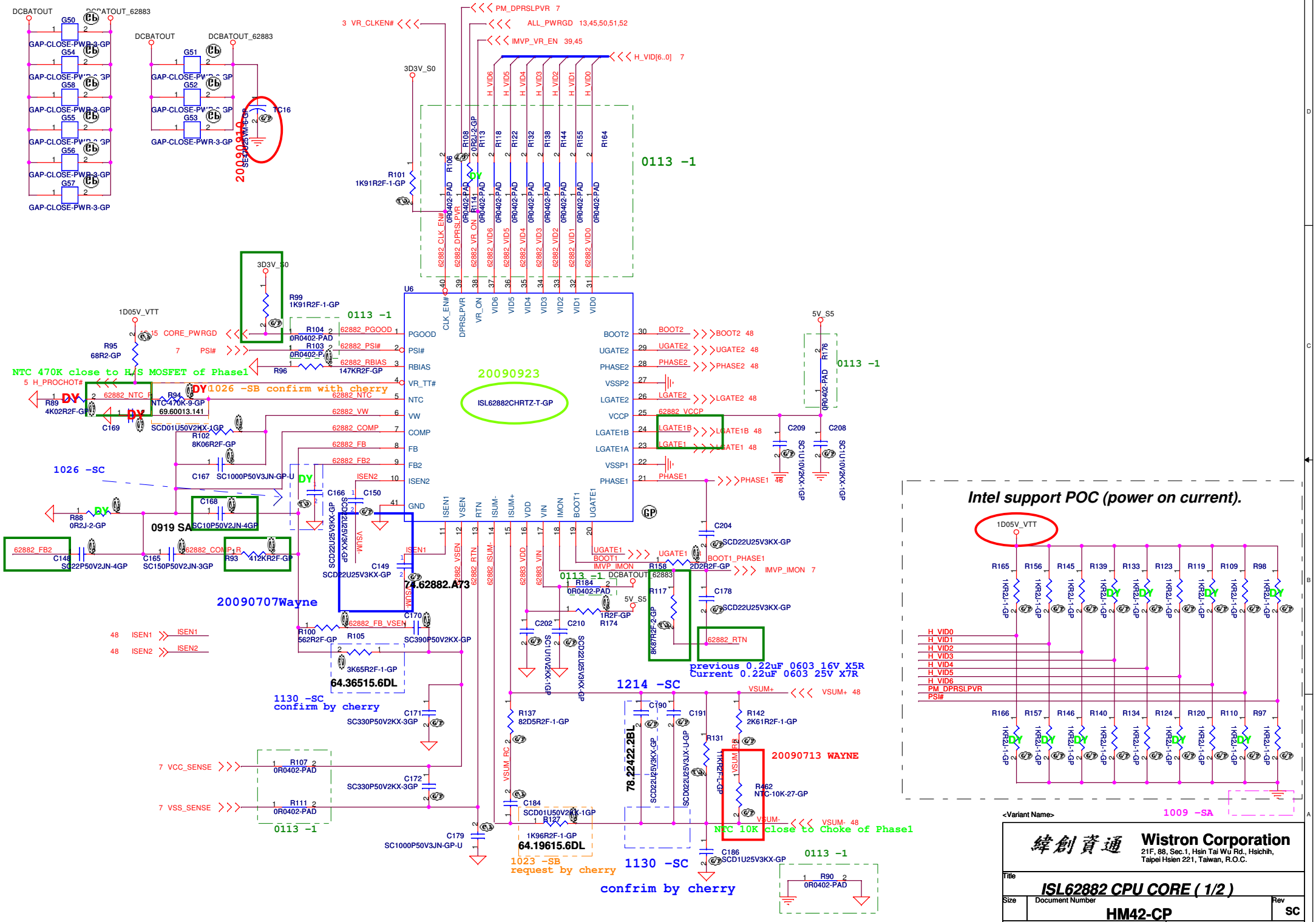
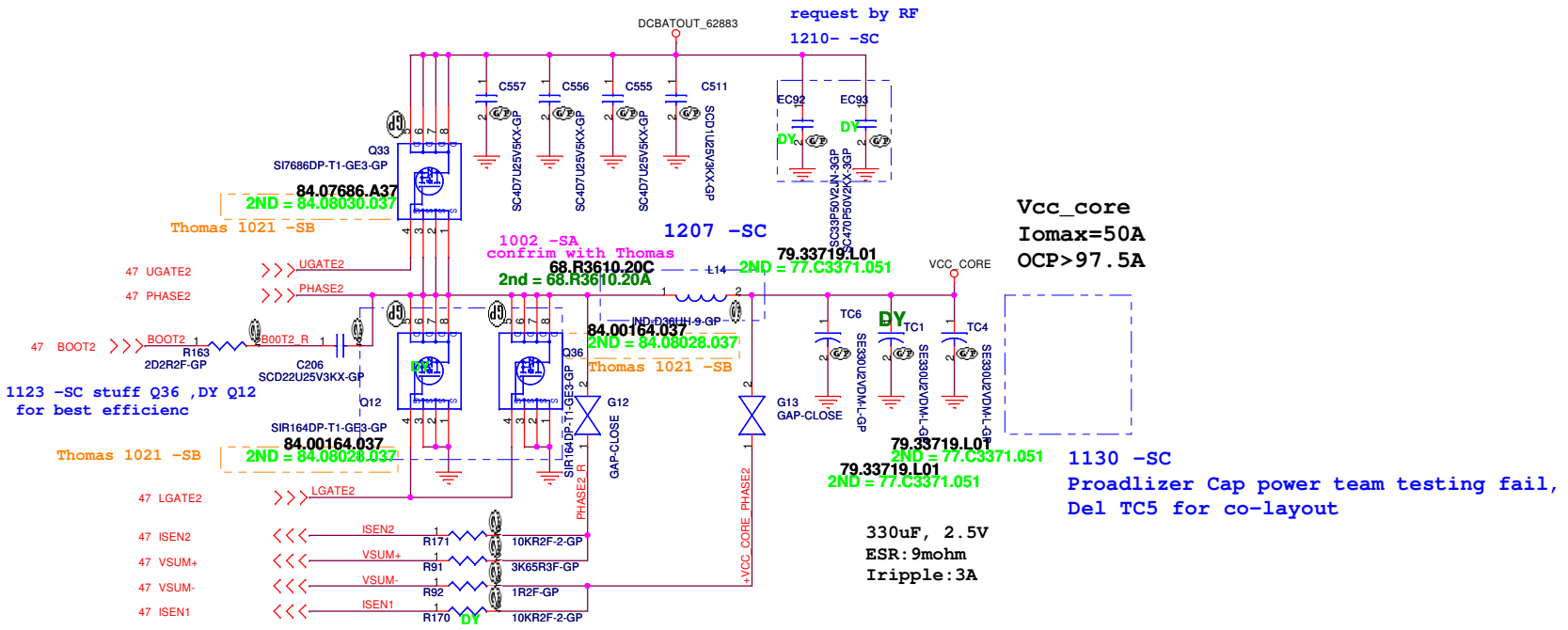
Taipei Hsien 221, Taiwan, R.O.C.

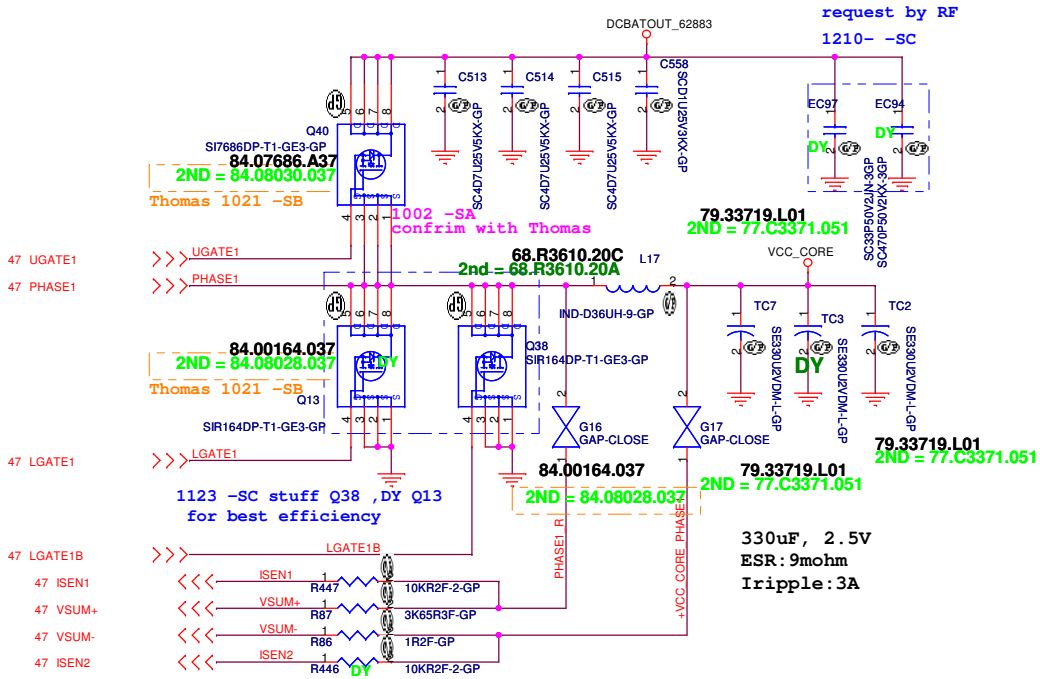
Title: **Power Block Diagram**

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 46 of 72


U6
ISL62882CHRTZ-GP
20090923
0113 -1
1026 -SB confirm with cherry
NTC 470K close to H/S MOSFET of Phase1
1026 -SC
0919 SA
20090707Wayne
74.62882.A73
64.36515.6DL
1130 -SC
confirm by cherry
1214 -SC
78.22422.2BL
20090713 WAYNE
NTC 10K close to Choke of Phase1
64.19615.6DL
1023 -SB
request by cherry
1130 -SC
confrim by cherry
previous 0.22uF 0603 16V X5R
Current 0.22uF 0603 25V X7R
Intel support POC (power on current).
1009 -SA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL62882 CPU CORE (1/2)
HM42-CP
Rev SC
Date: Friday, January 22, 2010
Sheet 47 of 72





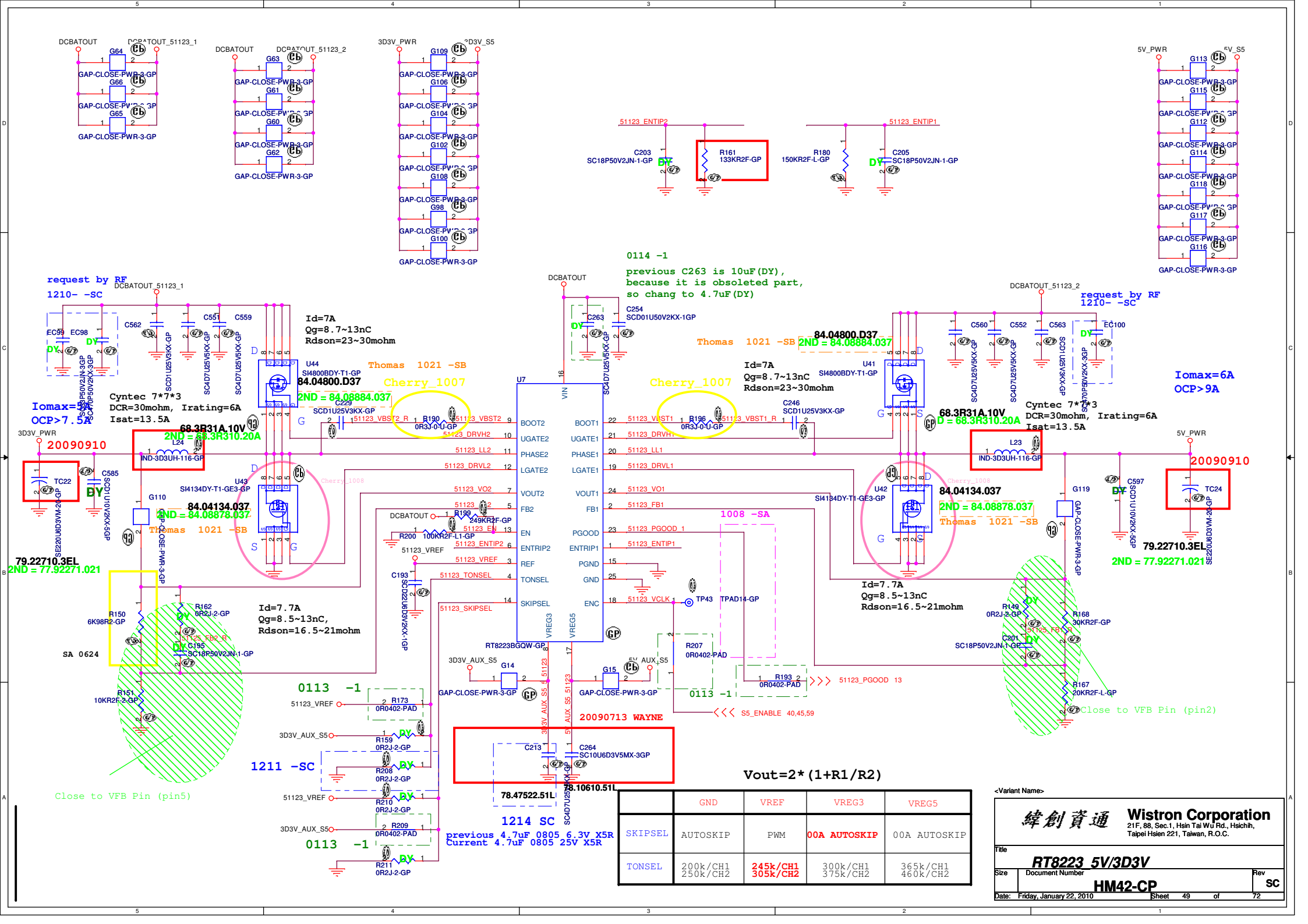
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62882 CPU CORE (1/2)

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 48 of 72



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

Size | Document Number: HM42-CP | Rev: SC

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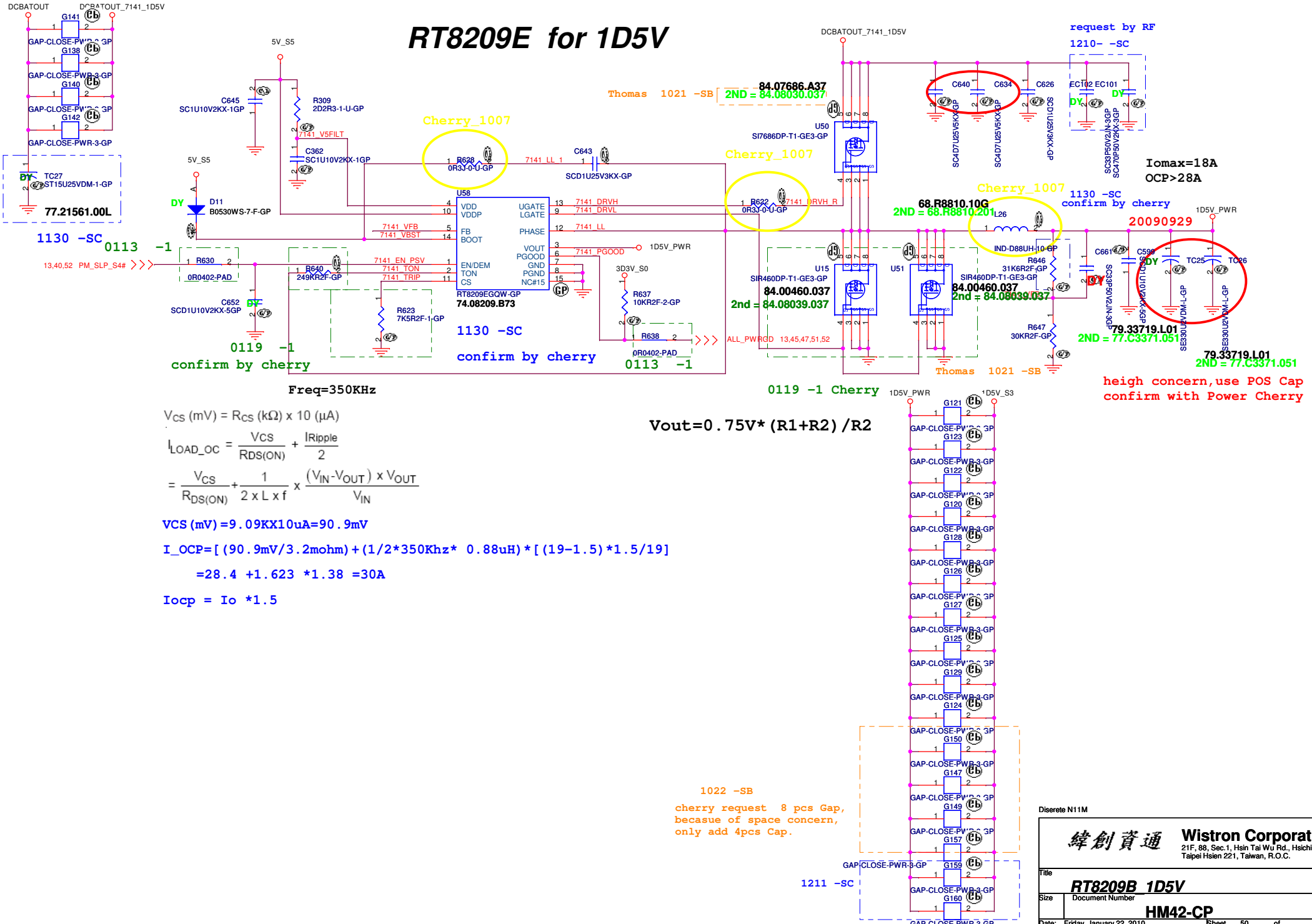
RT8209E for 1D5V



$$V_{CS}\,(mV) = R_{CS}\,(k\Omega) \times 10\,(\mu A)$$

$$I_{LOAD\_OC} = \frac{V_{CS}}{R_{DS(ON)}} + \frac{I_{Ripple}}{2}$$

$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{V_{IN}}$$

VCS(mV)=9.09KX10uA=90.9mV

I_OCP=[(90.9mV/3.2mohm)+(1/2*350Khz* 0.88uH)*[(19-1.5)*1.5/19]

=28.4 +1.623 *1.38 =30A

Iocp = Io *1.5

Diserete N11M

緯創資通 Wistron Corporation
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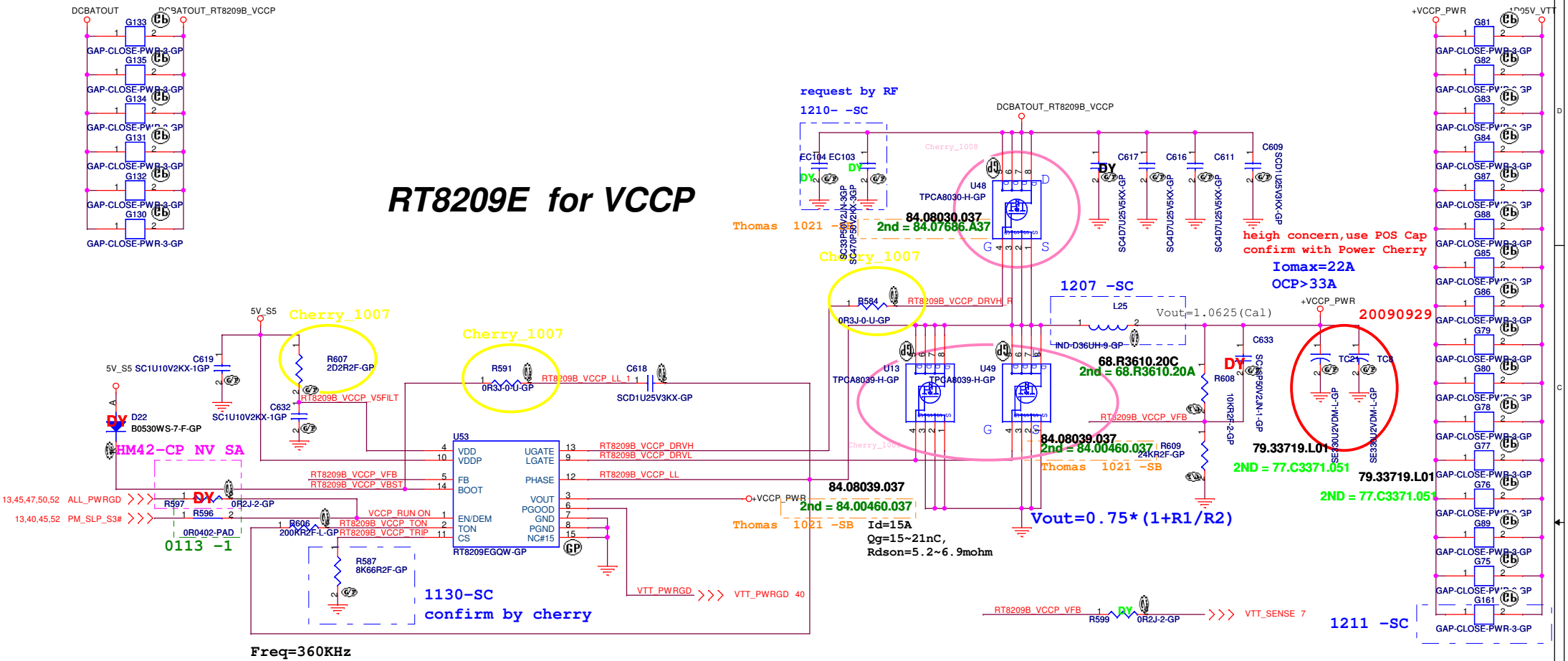
Title: RT8209B 1D5V

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 50 of 72

RT8209E for VCCP



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: RT8209B +VCCP	
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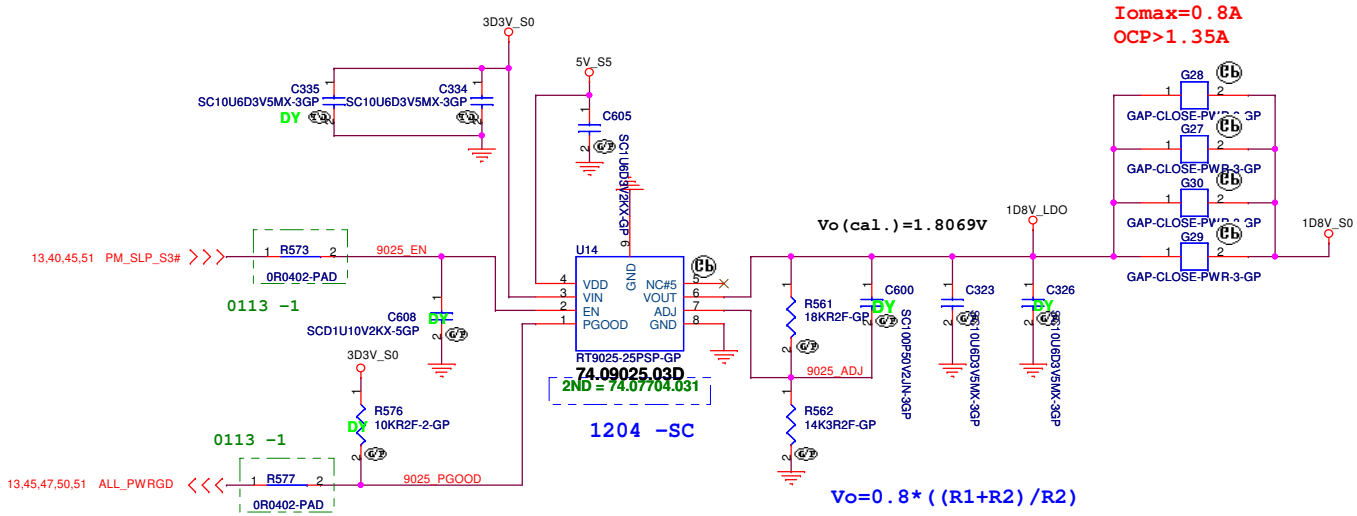
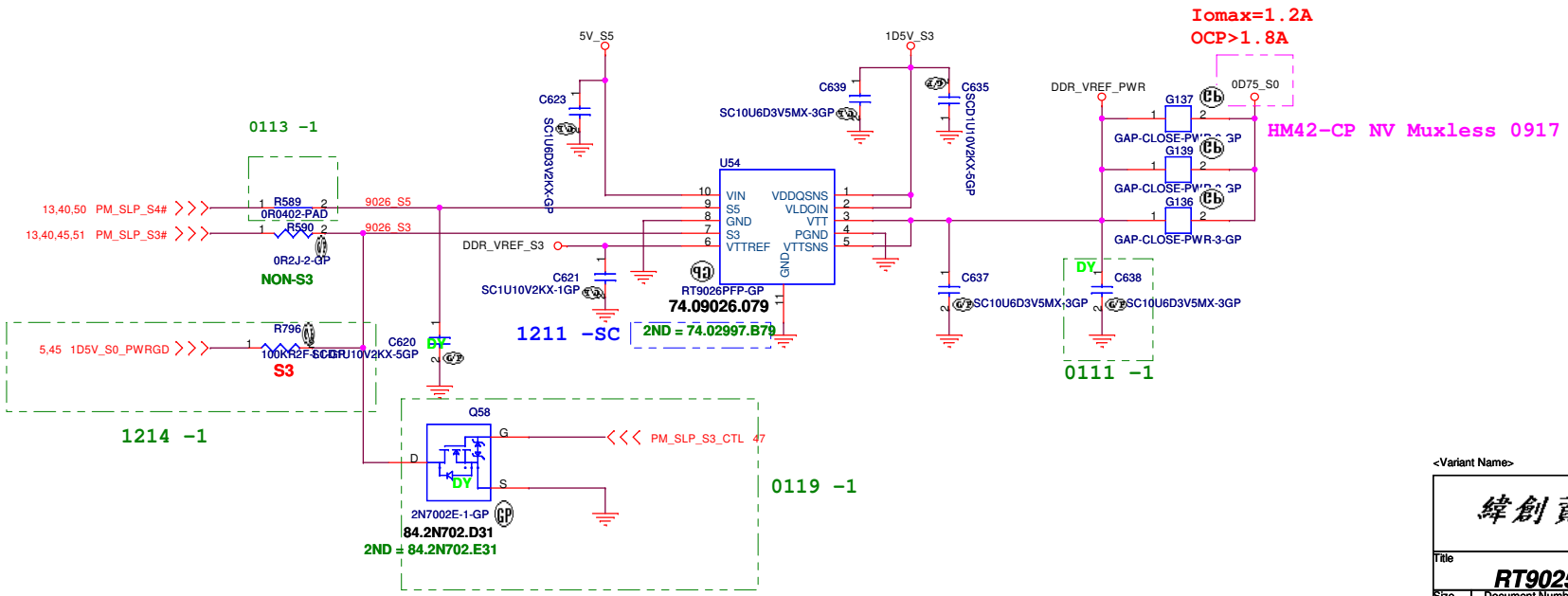
Date: Friday, January 22, 2010	Sheet 51 of 72

RT9025 for 1D8V_S0

20090915



RT9026 for 0D75V_S0



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_1D8V/RT9026_0D75

Size | Document Number: HM42-CP | Rev: SC

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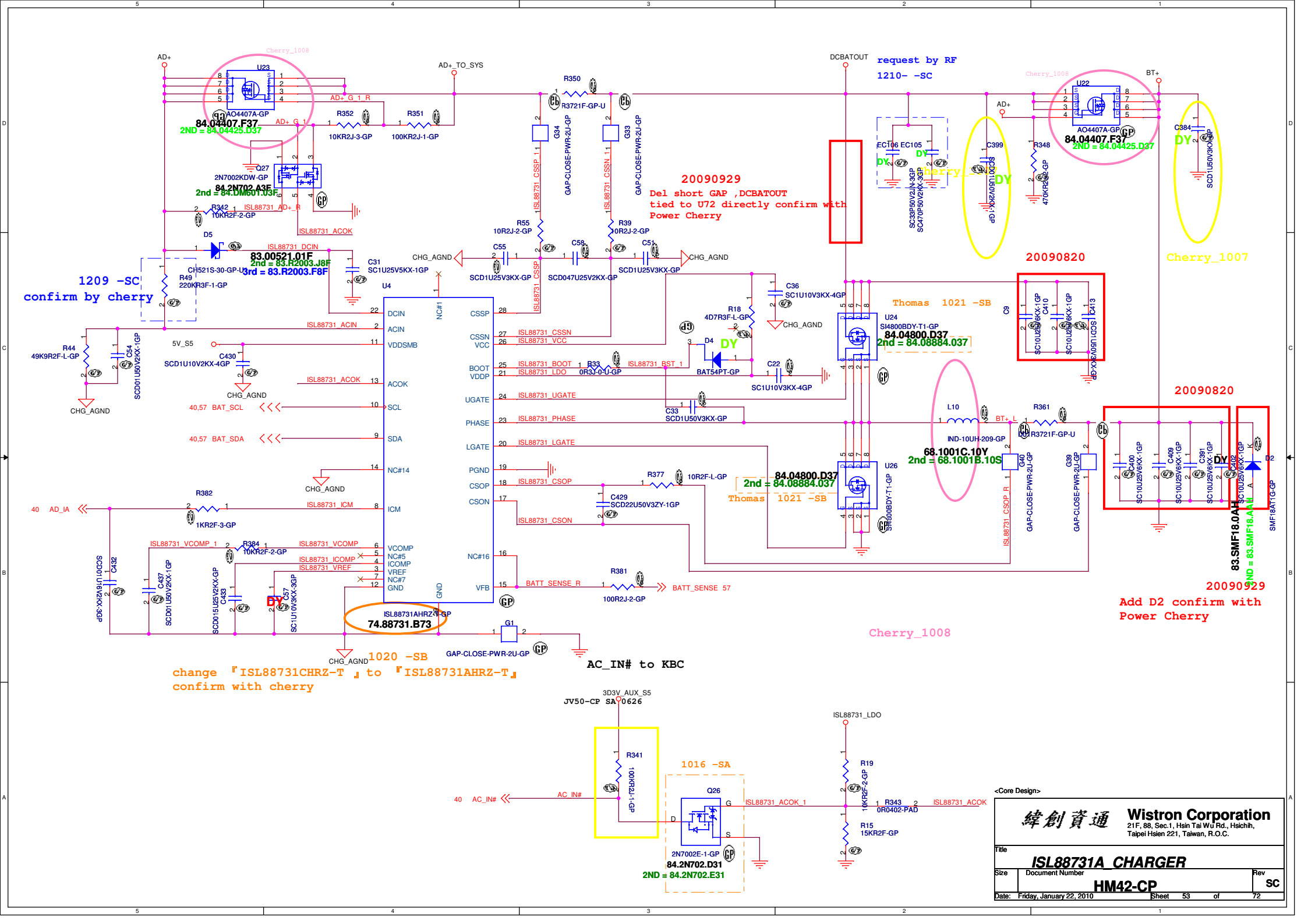
AD+
AD+_TO_SYS
DCBATOUT
request by RF
1210- -SC
BT+
U23
AO4407A-GP
84.04407.F37
2ND = 84.04425.D37
AD+_G_1_R
AD+_G_1
R352
10KR2J-3-GP
R351
100KR2J-1-GP
R350
R3721F-GP-U
G34
GAP-CLOSE-PWR-2U-GP
G33
GAP-CLOSE-PWR-2U-GP
ISL88731_CSSP_1
ISL88731_CSSN_1
Q27
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
R342
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
D5
CH521S-30-GP-U
ISL88731_DCIN
83.00521.01F
2nd = 83.R2003.J8F
3rd = 83.R2003.F8F
R49
220KR3F-1-GP
1209 -SC
confirm by cherry
C31
SC1U25V5KX-1GP
U4
CHG_AGND
R55
10R2J-2-GP
R39
10R2J-2-GP
C55
SCD1U25V3KX-GP
C58
SCD047U25V2KX-GP
C51
SCD1U25V3KX-GP
20090929
Del short GAP ,DCBATOUT
tied to U72 directly confirm with
Power Cherry
EC106 EC105
DY
SC33P50V2JN-3GP
SC470P50V2KX-3GP
C399
SCD1U50V2KX-1GP
DY
Cherry_1008
U22
AO4407A-GP
84.04407.F37
2ND = 84.04425.D37
R348
470KR2J-2-GP
C384
SCD1U50V3KX-GP
DY
Cherry_1007
20090820
Thomas 1021 -SB
U24
SI4800BDY-T1-GP
84.04800.D37
2nd = 84.08884.037
C9
SC10U25V6KX-1GP
C410
SC10U25V6KX-1GP
C413
SCD1U50V3KX-GP
C36
SC1U10V3KX-4GP
R18
4D7R3F-L-GP
D4
DY
BAT54PT-GP
C22
SC1U10V3KX-4GP
C33
SCD1U50V3KX-GP
L10
IND-10UH-209-GP
68.1001C.10Y
2nd = 68.1001B.10S
R361
0R3R3721F-GP-U
U26
SI4800BDY-T1-GP
84.04800.D37
2nd = 84.08884.037
Thomas 1021 -SB
G40
GAP-CLOSE-PWR-2U-GP
G39
GAP-CLOSE-PWR-2U-GP
ISL88731_CSOP_R
C400
SC10U25V6KX-1GP
C409
SC10U25V6KX-1GP
C391
SC10U25V6KX-1GP
DY
C402
SC10U25V6KX-1GP
D2
SMF18ATT-GP
83.SMF18.AAH
2ND = 83.SMF18.AAH
20090820
20090929
Add D2 confirm with
Power Cherry
R44
49K9R2F-L-GP
C54
SCD01U50V2KX-1GP
5V_S5
C430
SCD1U10V2KX-4GP
CHG_AGND
ISL88731_ACIN
ISL88731_ACOK
40,57 BAT_SCL
40,57 BAT_SDA
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#1
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_BST_1
R33
0R3J-0-U-GP
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
R377
10R2F-L-GP
C429
SCD22U50V3ZY-1GP
R382
1KR2F-3-GP
40 AD_IA
ISL88731_ICM
ISL88731_VCOMP_1
R384
10KR2F-2-GP
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
C482
SCD01U50V2KX-3GP
C437
SCD01U50V2KX-1GP
SCD015U25V2KX-GP
C433
C57
SC1U10V3KX-3GP
DY
ISL88731AHRZ-T-GP
74.88731.B73
R381
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 57
G1
GAP-CLOSE-PWR-2U-GP
CHG_AGND
1020 -SB
change 『ISL88731CHRZ-T 』to 『ISL88731AHRZ-T』
confirm with cherry
AC_IN# to KBC
Cherry_1008
3D3V_AUX_S5
JV50-CP SA10626
R341
100KR2J-1-GP
40 AC_IN#
AC_IN#
1016 -SA
Q26
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
ISL88731_LDO
R19
10KR2F-2-GP
R343
0R0402-PAD
ISL88731_ACOK_1
ISL88731_ACOK
R15
15KR2F-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_CHARGER
Size
Document Number
HM42-CP
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SC
Date: Friday, January 22, 2010
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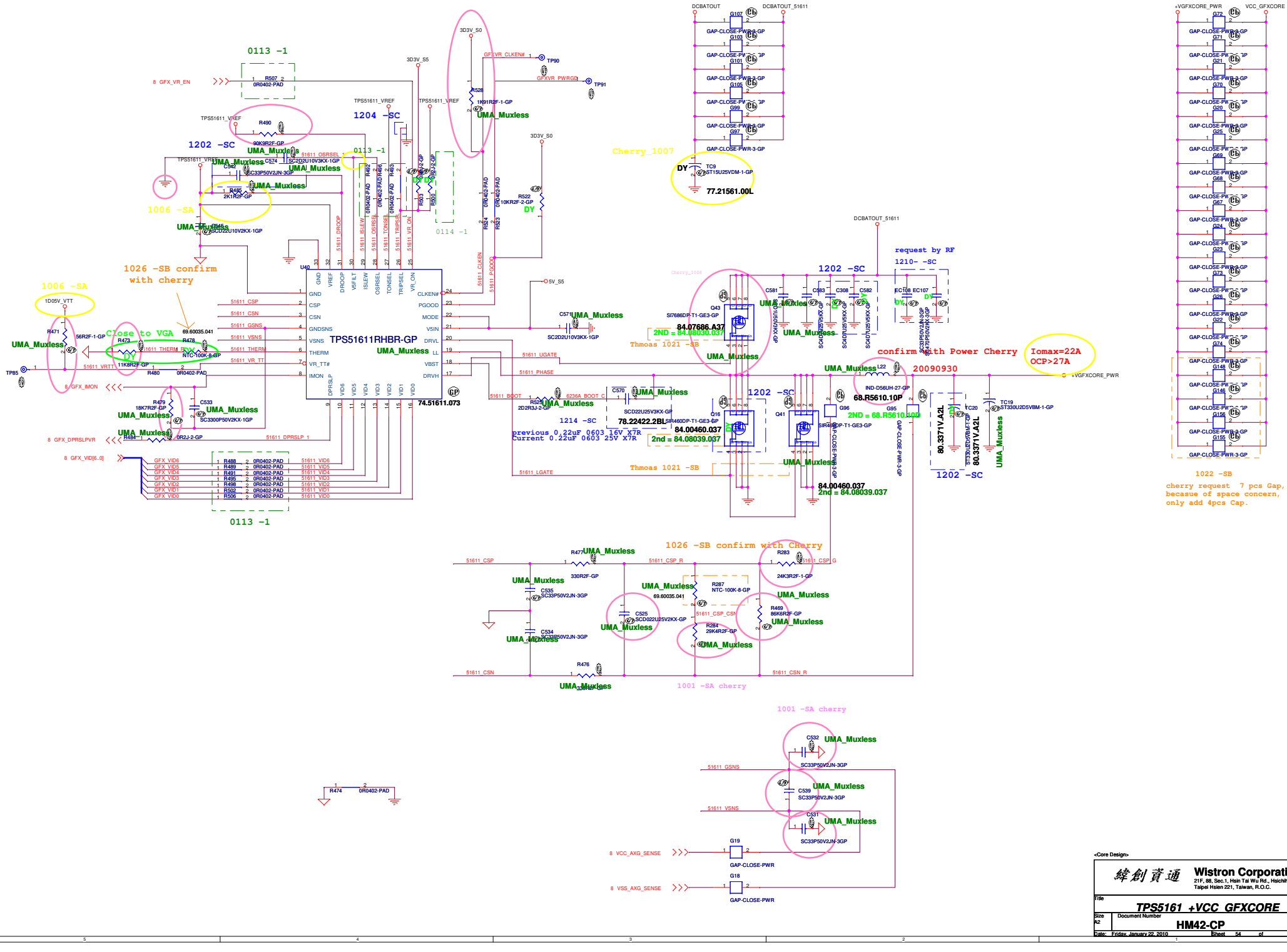
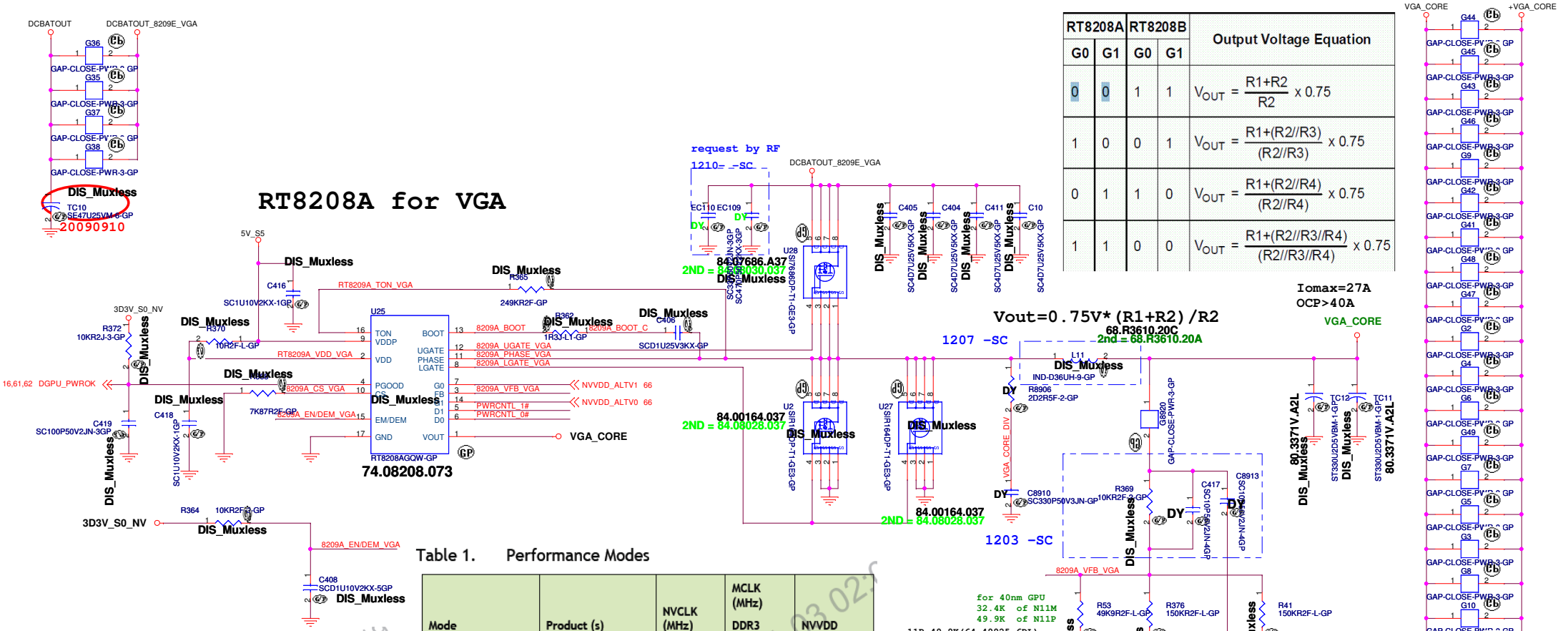

0113 -1
1204 -SC
1202 -SC
1006 -SA
1026 -SB confirm with cherry
Close to VGA
TPS51611RHBR-GP
74.51611.073
Cherry_1007
77.21561.00L
request by RF
1210- -SC
confirm with Power Cherry
Iomax=22A
OCP>27A
20090930
68.R5610.10P
84.07686.A37
84.00460.037
2nd = 84.08039.037
1214 -SC
previous 0.22uF 0603 16V X7R
Current 0.22uF 0603 25V X7R
1001 -SA cherry
1022 -SB
cherry request 7 pcs Gap, becasue of space concern, only add 4pcs Cap.
UMA_Muxless
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
TPS5161 +VCC_GFXCORE
HM42-CP
SC
Friday, January 22, 2010

RT8208A for VGA



RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11P-OP1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-OP1, N11M-OP2	405	405	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1, N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1, N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1, N11M-LP1	135	135	0.85 V

N11P-GE1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5//NVVDD_ALTV0	NVVDD
0	0	0.8
0	1	0.85
1	0	0.95

N11M-GE1/N11M-OP1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5/NVVDD_ALTV0	NVVDD
0	1	0.85
1	0	1.03

UMA

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209A_VGA_CORE

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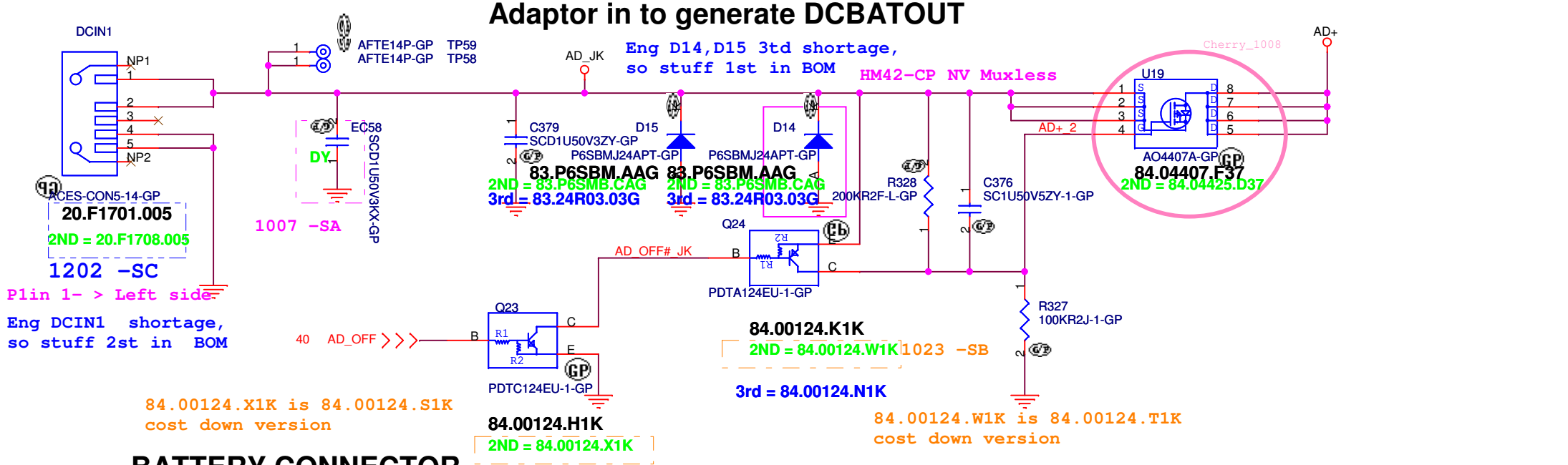
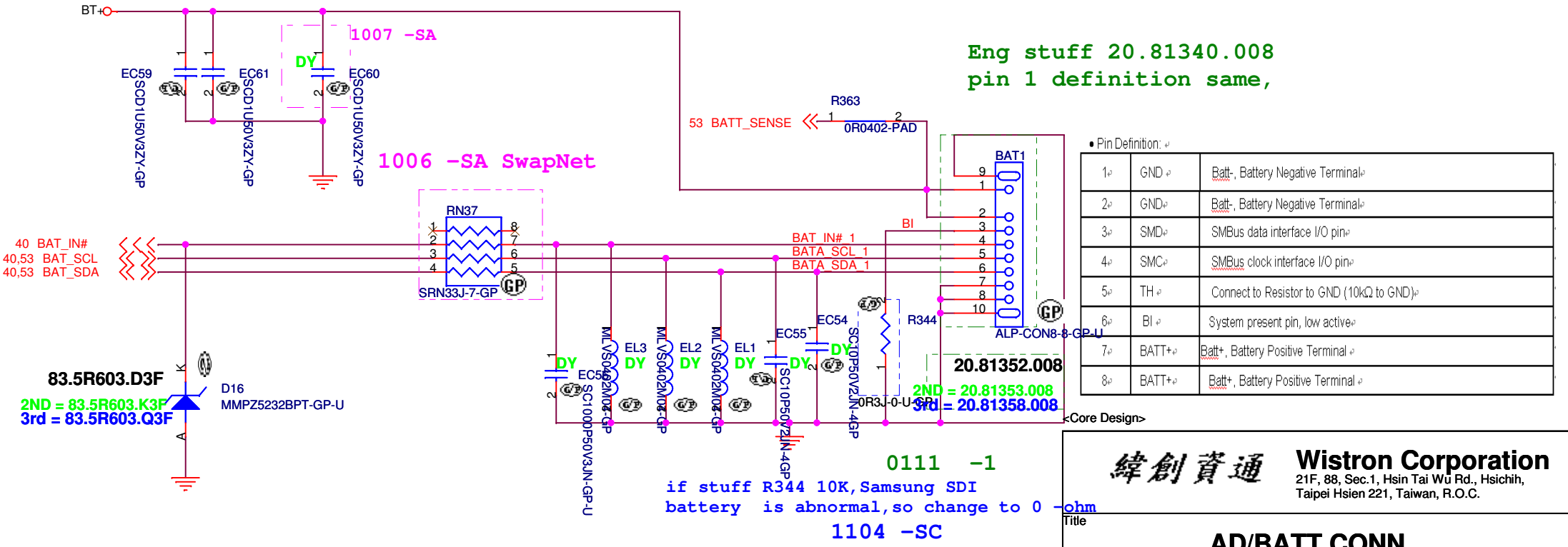
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

<Core Design>

緯創資通 **Wistron Corporation**
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Title: **AD/BATT CONN**

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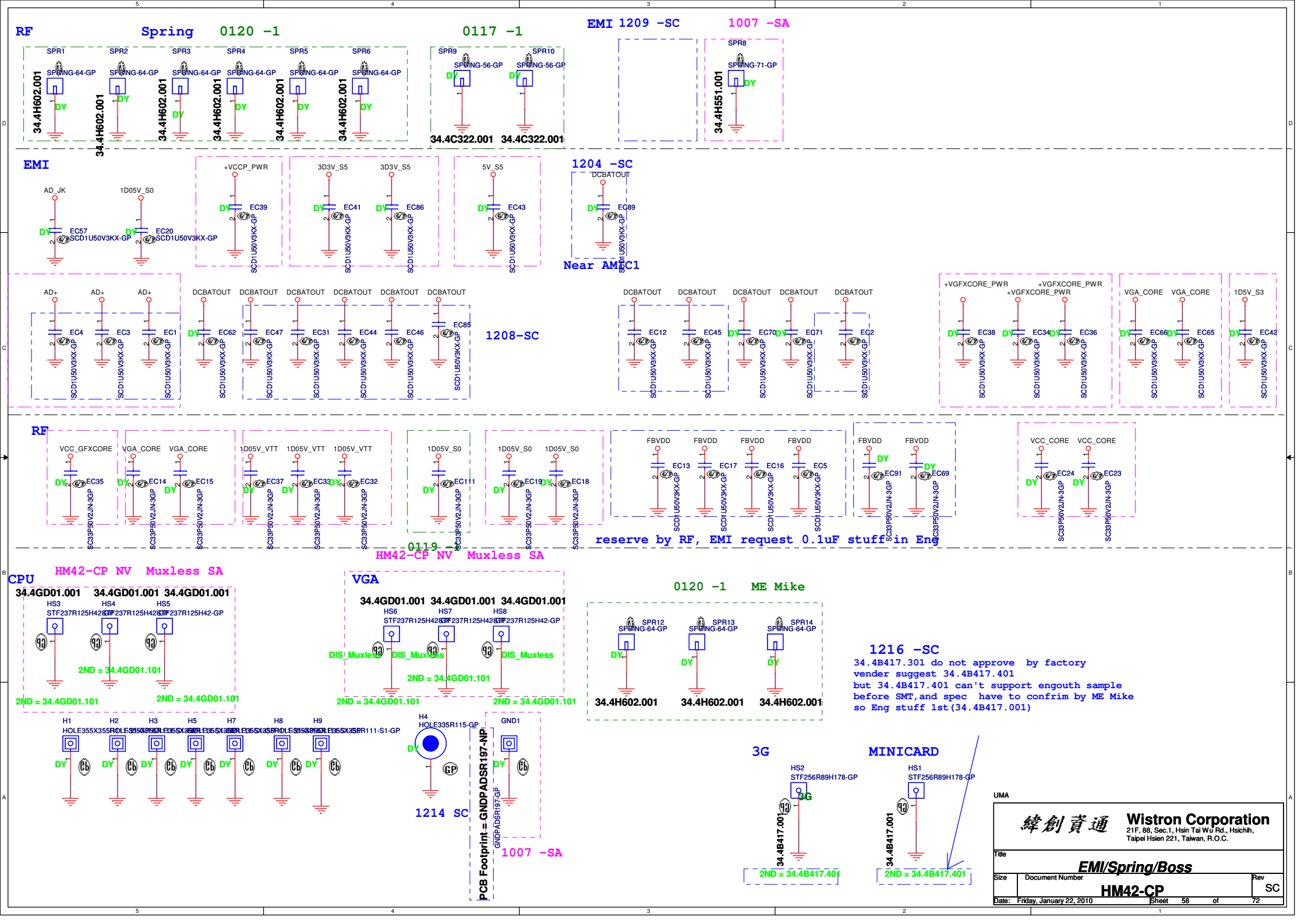
RF
Spring
0120 -1
0117 -1
EMI 1209 -SC
1007 -SA
SPR1
SPR2
SPR3
SPR4
SPR5
SPR6
SPRING-64-GP
34.4H602.001
DY
SPR9
SPR10
SPRING-56-GP
34.4C322.001
SPR8
SPRING-71-GP
34.4H551.001
EMI
AD_JK
1D05V_S0
EC57
EC20
SCD1U50V3KX-GP
+VCCP_PWR
EC39
3D3V_S5
EC41
EC86
5V_S5
EC43
1204 -SC
DCBATOUT
EC89
Near AMEC1
AD+
EC4
EC3
EC1
EC62
EC47
EC31
EC44
EC46
EC85
1208-SC
EC12
EC45
EC70
EC71
EC2
+VGFXCORE_PWR
EC38
EC34
EC36
VGA_CORE
EC66
EC65
1D5V_S3
EC42
RF
VCC_GFXCORE
EC35
EC14
EC15
1D05V_VTT
EC37
EC33
EC32
EC111
EC19
EC18
FBVDD
EC13
EC17
EC16
EC5
EC91
EC69
VCC_CORE
EC24
EC23
SC33P50V2JN-3GP
0119 -2
HM42-CP NV Muxless SA
reserve by RF, EMI request 0.1uF stuff in Eng
CPU
34.4GD01.001
HS3
HS4
HS5
STF237R125H42-GP
2ND = 34.4GD01.101
VGA
HS6
HS7
HS8
DIS_Muxless
0120 -1 ME Mike
SPR12
SPR13
SPR14
34.4H602.001
1216 -SC
34.4B417.301 do not approve by factory
vender suggest 34.4B417.401
but 34.4B417.401 can't support engouth sample
before SMT,and spec have to confrim by ME Mike
so Eng stuff 1st(34.4B417.001)
H1
H2
H3
H5
H7
H8
H9
HOLE355X355R111-S1-GP
CB
H4
HOLE335R115-GP
GP
GND1
1214 SC
PCB Footprint = GNDPADSR197-NP
GNDPADSR197-GP
1007 -SA
3G
MINICARD
HS2
HS1
STF256R89H178-GP
34.4B417.001
2ND = 34.4B417.401
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
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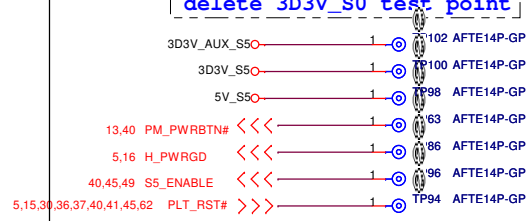
Check test point

delete 3D3V_S0 test point



Test Point放在Dimm Door打開可量測處

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AFTE_TP***

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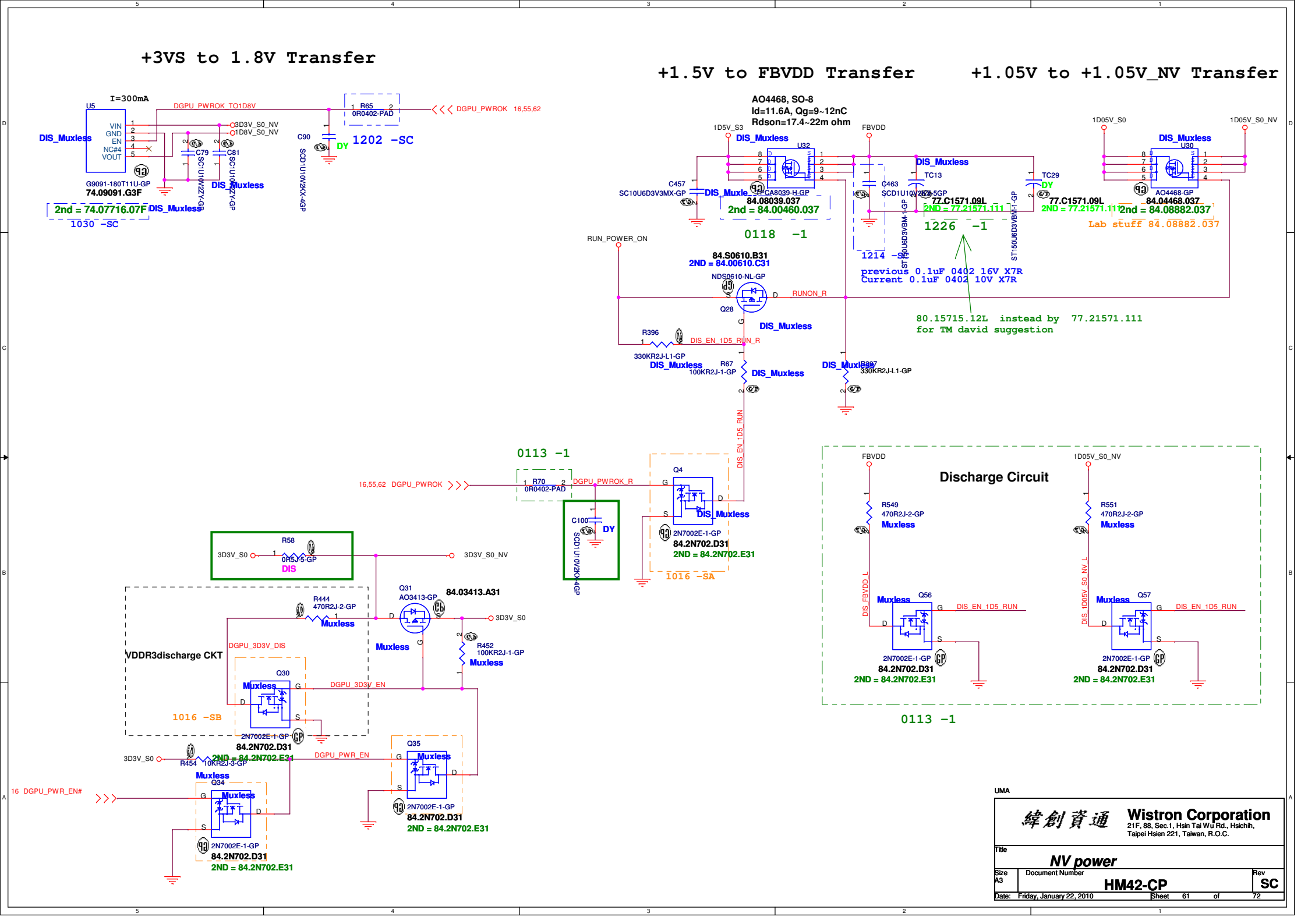
+3VS to 1.8V Transfer
+1.5V to FBVDD Transfer
+1.05V to +1.05V_NV Transfer
I=300mA
U5
VIN
GND
EN
NC#4
VOUT
DIS_Muxless
G9091-180T11U-GP
74.09091.G3F
2nd = 74.07716.07F
1030 -SC
DGPU_PWROK_TO1D8V
3D3V_S0_NV
1D8V_S0_NV
C79
C81
SC1U10V2Y-GP
C90
SCD1U10V2KX-4GP
DY
1202 -SC
R65
0R0402-PAD
DGPU_PWROK 16,55,62
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm
1D5V_S3
FBVDD
U32
C457
SC10U6D3V3MX-GP
CA8039-H-GP
84.08039.037
2nd = 84.00460.037
0118 -1
C463
SCD1U10V2KX-5GP
TC13
TC29
77.C1571.09L
2ND = 77.21571.111
1226 -1
ST150U6D3VBM-1-GP
1214 -SC
previous 0.1uF 0402 16V X7R
Current 0.1uF 0402 10V X7R
80.15715.12L instead by 77.21571.111
for TM david suggestion
1D05V_S0
1D05V_S0_NV
U30
AO4468-GP
84.04468.037
2nd = 84.08882.037
Lab stuff 84.08882.037
RUN_POWER_ON
84.S0610.B31
2ND = 84.00610.C31
NDS0610-NL-GP
Q28
RUNON_R
R396
330KR2J-L1-GP
DIS_EN_1D5_RUN_R
R67
100KR2J-1-GP
R397
330KR2J-L1-GP
DIS_EN_1D5_RUN
0113 -1
16,55,62 DGPU_PWROK
R70
0R0402-PAD
DGPU_PWROK_R
C100
SCD1U10V2KX-4GP
Q4
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
1016 -SA
Discharge Circuit
FBVDD
1D05V_S0_NV
R549
470R2J-2-GP
Muxless
R551
470R2J-2-GP
DIS_FBVDD_L
DIS_1D05V_S0_NV_L
Q56
Q57
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
0113 -1
R58
3D3V_S0
0R0J-S-GP
DIS
3D3V_S0_NV
VDDR3discharge CKT
Q31
AO3413-GP
84.03413.A31
R444
470R2J-2-GP
R452
100KR2J-1-GP
DGPU_3D3V_DIS
Q30
DGPU_3D3V_EN
1016 -SB
R454
10KR2J-3-GP
DGPU_PWR_EN
Q34
Q35
16 DGPU_PWR_EN#
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NV power
Size
A3
Document Number
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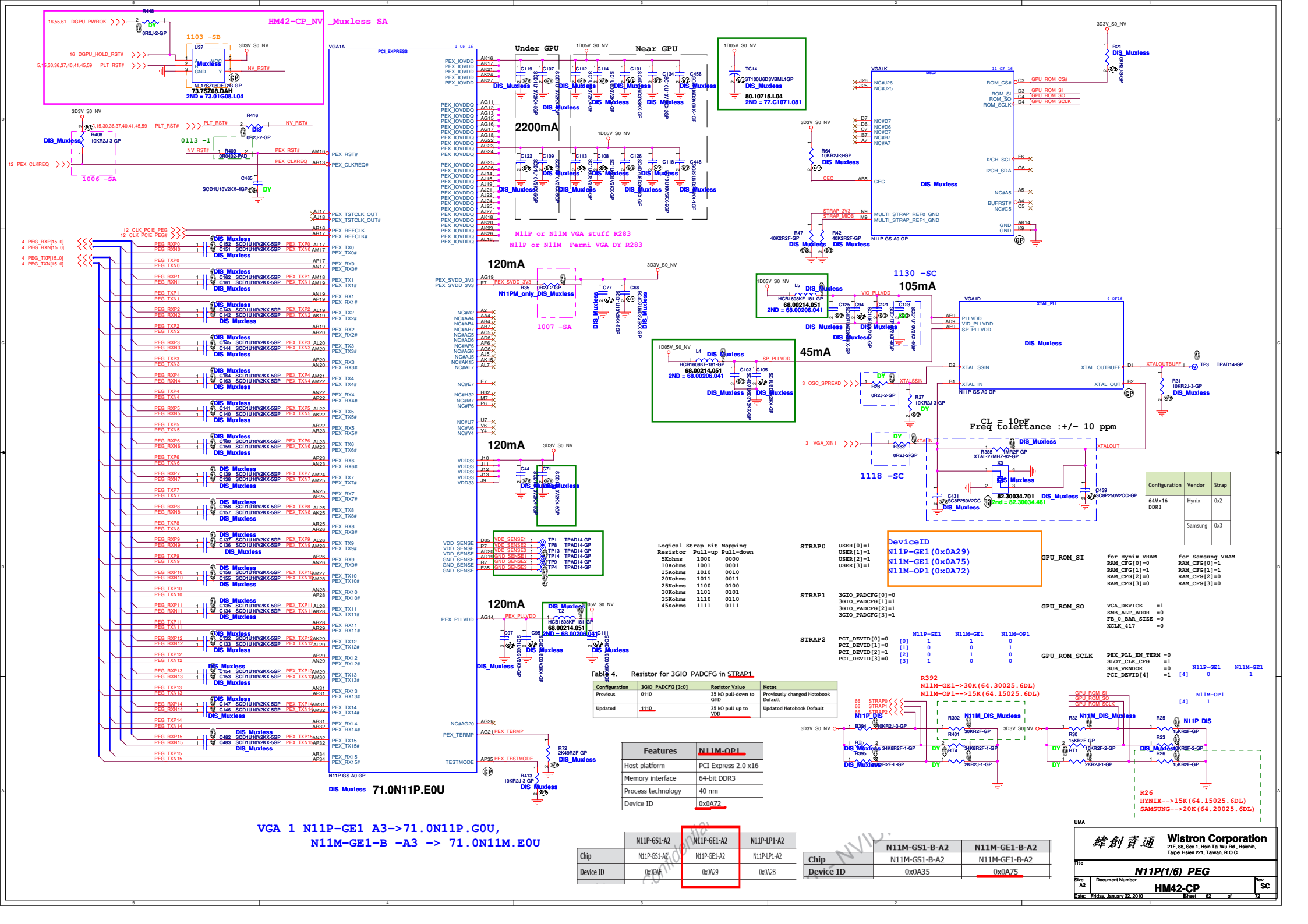

Configuration	Vendor	Strap
64M×16 DDR3	Hynix	0x2
	Samsung	0x3

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

STRAP0

USER[0]=1	
USER[1]=1	
USER[2]=1	
USER[3]=1	

STRAP1

3GIO_PADCFG[0]=0	
3GIO_PADCFG[1]=1	
3GIO_PADCFG[2]=1	
3GIO_PADCFG[3]=1	

STRAP2

	N11P-GE1	N11M-GE1	N11M-OP1
PCI_DEVID[0]=0 [0]	1	1	0
PCI_DEVID[1]=0 [1]	0	0	1
PCI_DEVID[2]=1 [2]	0	1	0
PCI_DEVID[3]=0 [3]	1	0	0

GPU_ROM_SI

for Hynix VRAM	for Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=0
RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO

VGA_DEVICE	=1
SMB_ALT_ADDR	=0
FB_0_BAR_SIZE	=0
XCLK_417	=0

GPU_ROM_SCLK

		N11P-GE1	N11M-GE1
PEX_PLL_EN_TERM	=0		
SLOT_CLK_CFG	=1		
SUB_VENDOR	=0		
PCI_DEVID[4]	=1	[4] 0	1

Table 4. Resistor for 3GIO_PADCFG in STRAP1

Configuration	3GIO_PADCFG [3:0]	Resistor Value	Notes
Previous	0110	35 kΩ pull-down to GND	Previously changed Notebook Default
Updated	1110	35 kΩ pull-up to VDD	Updated Notebook Default

Features	N11M-OP1
Host platform	PCI Express 2.0 x16
Memory interface	64-bit DDR3
Process technology	40 nm
Device ID	0x0A72

	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Chip	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Device ID	0x0CA0	0x0A29	0x0A2B

	N11M-GS1-B-A2	N11M-GE1-B-A2
Chip	N11M-GS1-B-A2	N11M-GE1-B-A2
Device ID	0x0A35	0x0A75

UMA

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Title: N11P(1/6)_PEG

Size: A2 | Document Number: HM42-CP | Rev: SC

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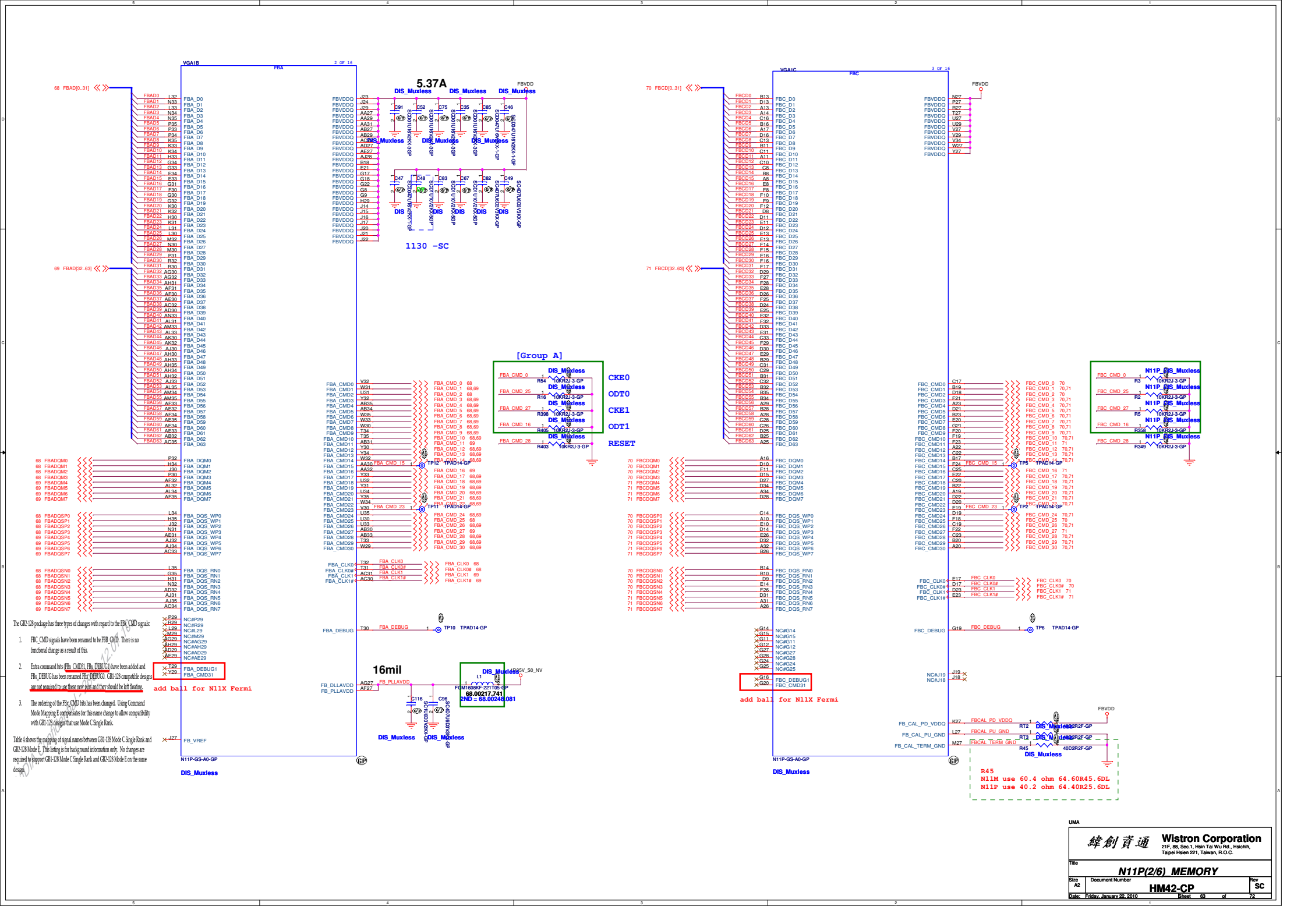

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Title: N11P(2/6)_MEMORY

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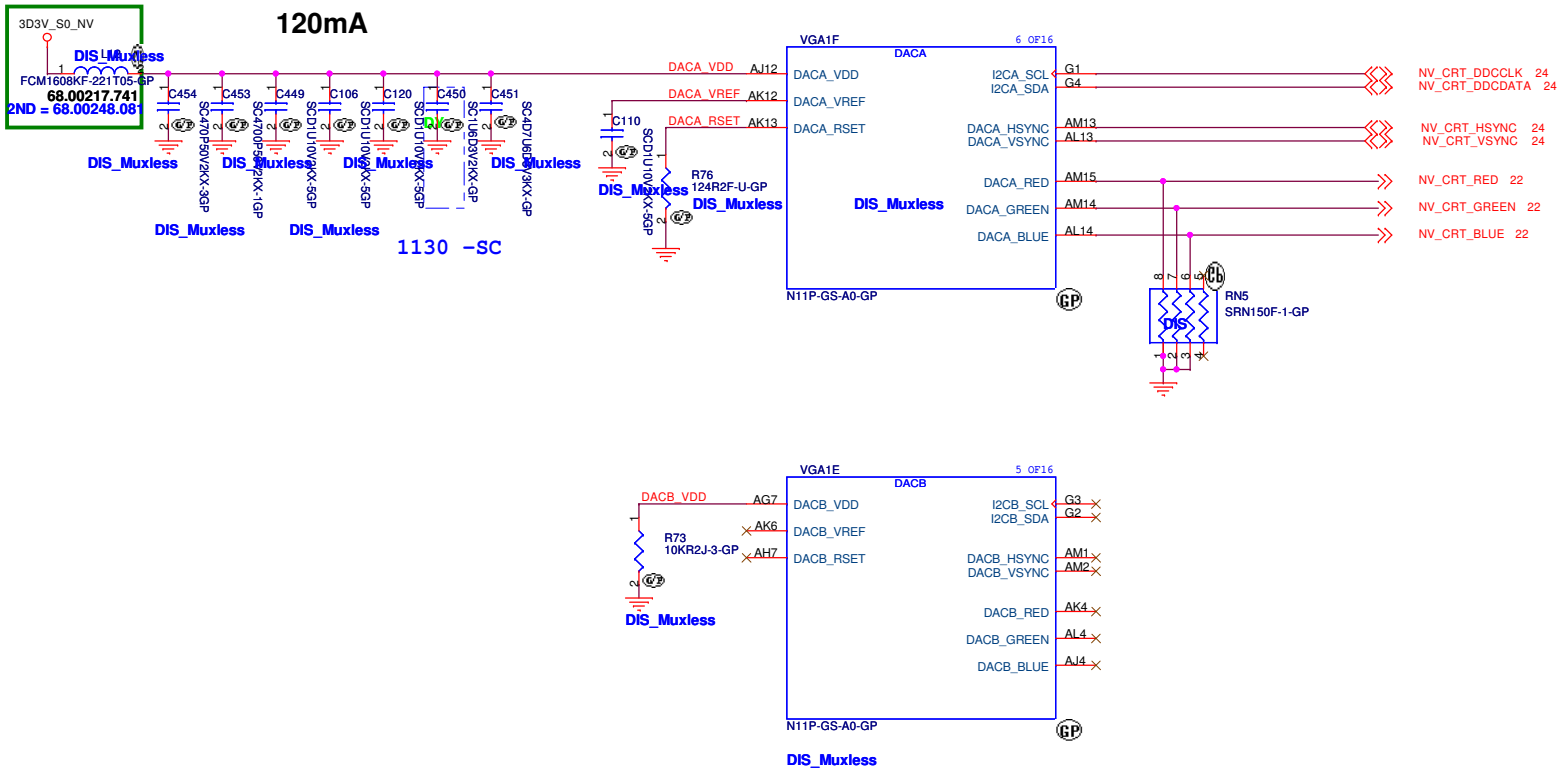

Diserete N11M

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Title: *N11P(3/6)_DAC*		
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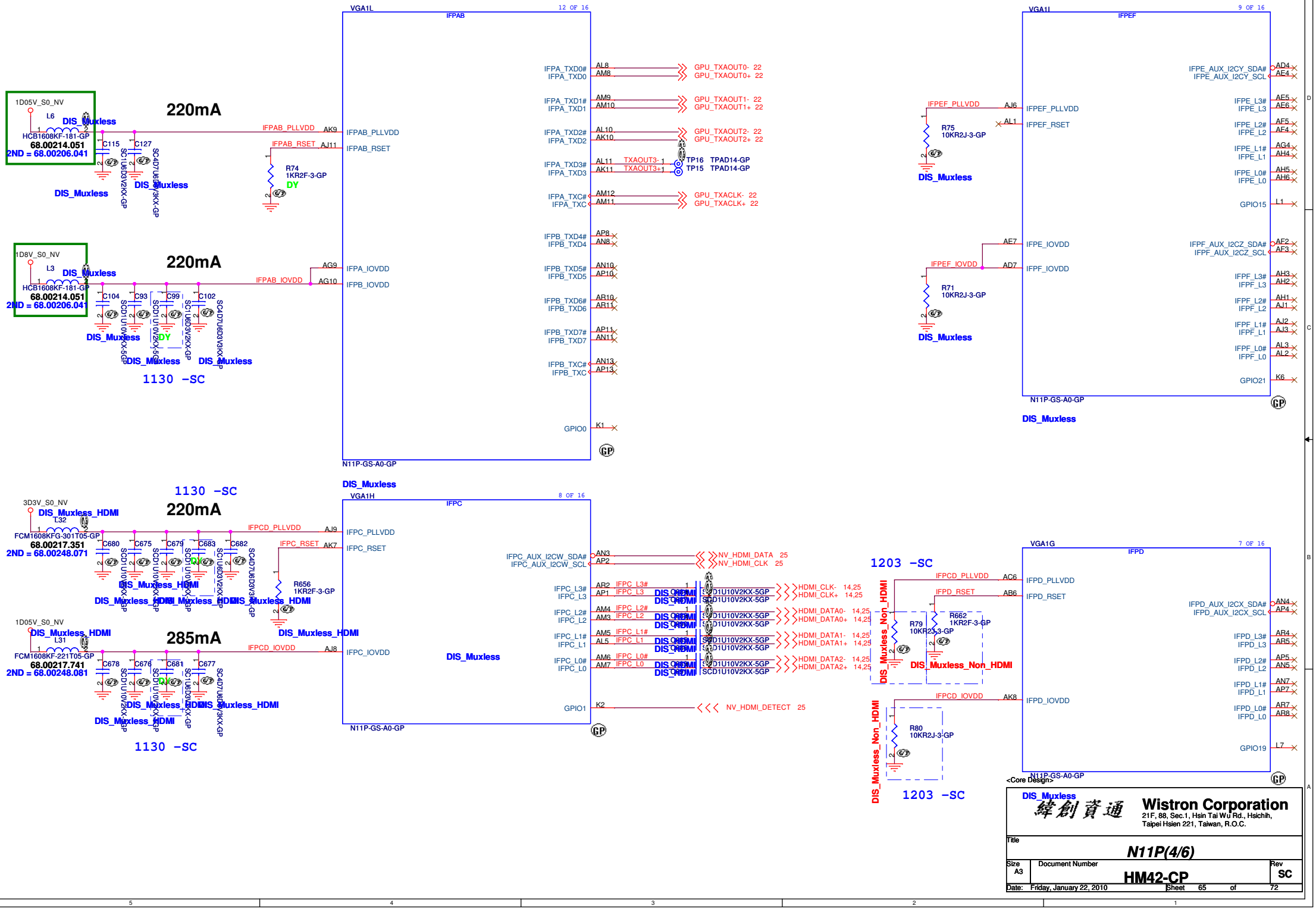
VGA1L
12 OF 16
IFPAB
N11P-GS-A0-GP
1D05V_S0_NV
220mA
L6
HCB1608KF-181-GP
68.00214.051
2ND = 68.00206.041
DIS_Muxless
IFPAB_PLLVDD
IFPAB_RSET
R74
1KR2F-3-GP
DY
1D8V_S0_NV
L3
IFPAB_IOVDD
IFPA_IOVDD
IFPB_IOVDD
1130 -SC
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPA_TXC#
IFPA_TXC
GPU_TXAOUT0- 22
GPU_TXAOUT0+ 22
GPU_TXAOUT1- 22
GPU_TXAOUT1+ 22
GPU_TXAOUT2- 22
GPU_TXAOUT2+ 22
TXAOUT3-
TXAOUT3+
TP16 TPAD14-GP
TP15 TPAD14-GP
GPU_TXACLK- 22
GPU_TXACLK+ 22
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
IFPB_TXC#
IFPB_TXC
GPIO0
VGA1H
8 OF 16
IFPC
3D3V_S0_NV
DIS_Muxless_HDMI
L32
FCM1608KFG-301T05-GP
68.00217.351
2ND = 68.00248.071
IFPCD_PLLVDD
IFPC_PLLVDD
IFPC_RSET
R656
1KR2F-3-GP
1D05V_S0_NV
L31
FCM1608KF-221T05-GP
68.00217.741
2ND = 68.00248.081
285mA
IFPCD_IOVDD
IFPC_IOVDD
1130 -SC
IFPC_AUX_I2CW_SDA#
IFPC_AUX_I2CW_SCL
IFPC_L3#
IFPC_L3
IFPC_L2#
IFPC_L2
IFPC_L1#
IFPC_L1
IFPC_L0#
IFPC_L0
NV_HDMI_DATA 25
NV_HDMI_CLK 25
HDMI_CLK- 14,25
HDMI_CLK+ 14,25
HDMI_DATA0- 14,25
HDMI_DATA0+ 14,25
HDMI_DATA1- 14,25
HDMI_DATA1+ 14,25
HDMI_DATA2- 14,25
HDMI_DATA2+ 14,25
GPIO1
NV_HDMI_DETECT 25
VGA1I
9 OF 16
IFPEF
N11P-GS-A0-GP
IFPEF_PLLVDD
IFPEF_RSET
R75
10KR2J-3-GP
IFPEF_IOVDD
R71
10KR2J-3-GP
IFPE_IOVDD
IFPF_IOVDD
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
IFPE_L3#
IFPE_L3
IFPE_L2#
IFPE_L2
IFPE_L1#
IFPE_L1
IFPE_L0#
IFPE_L0
GPIO15
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
IFPF_L3#
IFPF_L3
IFPF_L2#
IFPF_L2
IFPF_L1#
IFPF_L1
IFPF_L0#
IFPF_L0
GPIO21
1203 -SC
VGA1G
7 OF 16
IFPD
N11P-GS-A0-GP
IFPCD_PLLVDD
IFPD_PLLVDD
IFPD_RSET
R662
1KR2F-3-GP
R79
10KR2J-3-GP
DIS_Muxless_Non_HDMI
IFPCD_IOVDD
R80
10KR2J-3-GP
IFPD_IOVDD
IFPD_AUX_I2CX_SDA#
IFPD_AUX_I2CX_SCL
IFPD_L3#
IFPD_L3
IFPD_L2#
IFPD_L2
IFPD_L1#
IFPD_L1
IFPD_L0#
IFPD_L0
GPIO19
<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
N11P(4/6)
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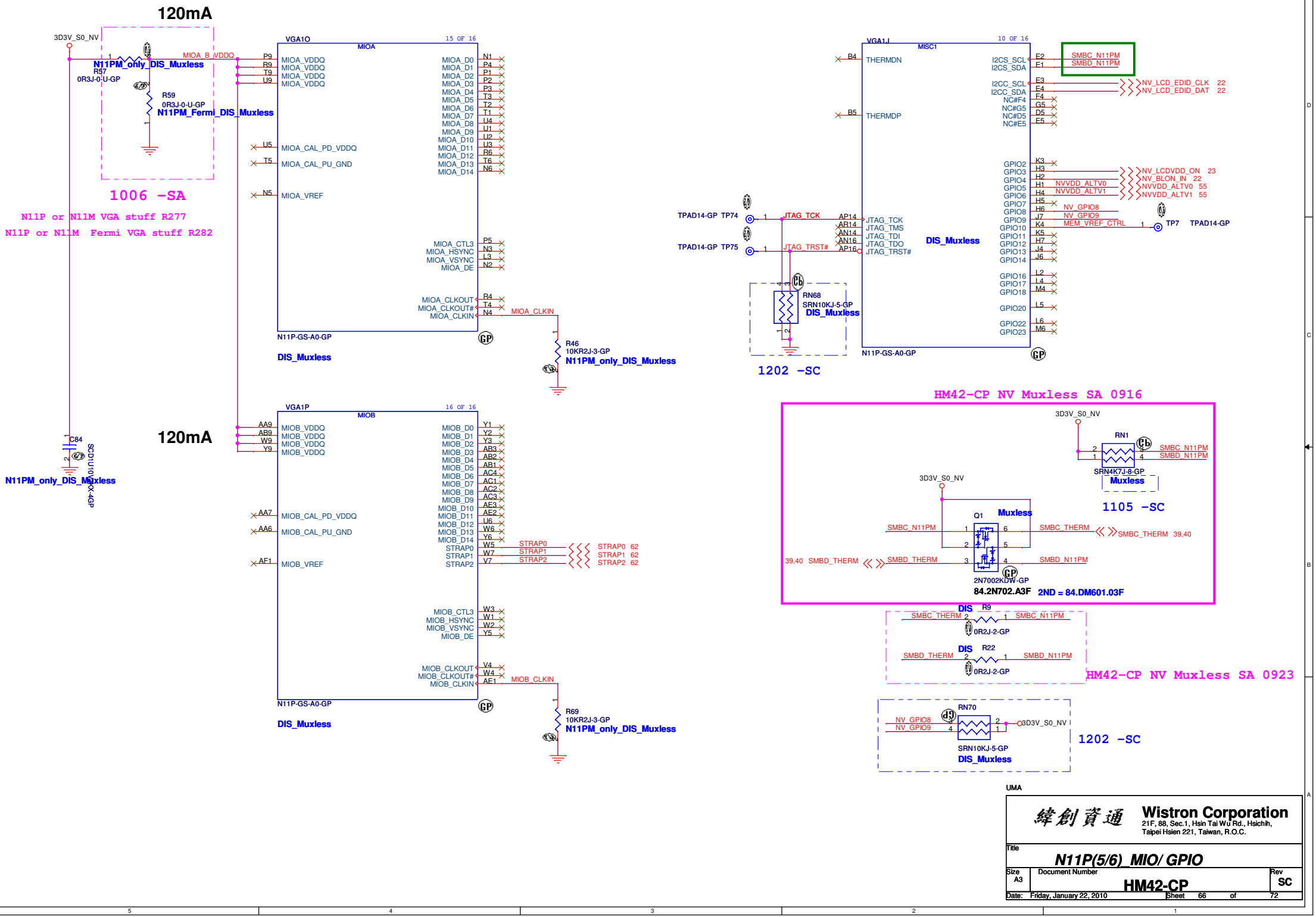

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***N11P(5/6)_MIO/ GPIO***	
Size: A3	Document Number: **HM42-CP**	Rev: SC
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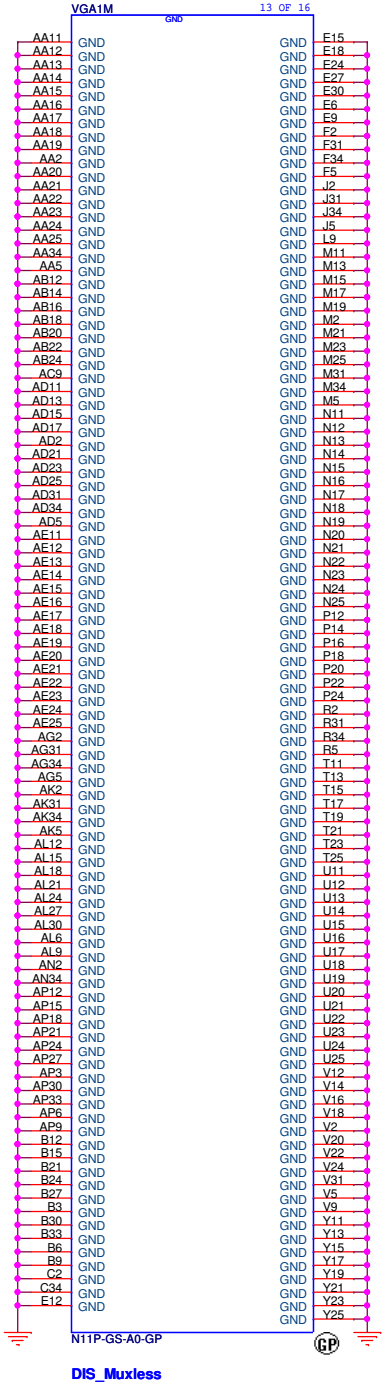

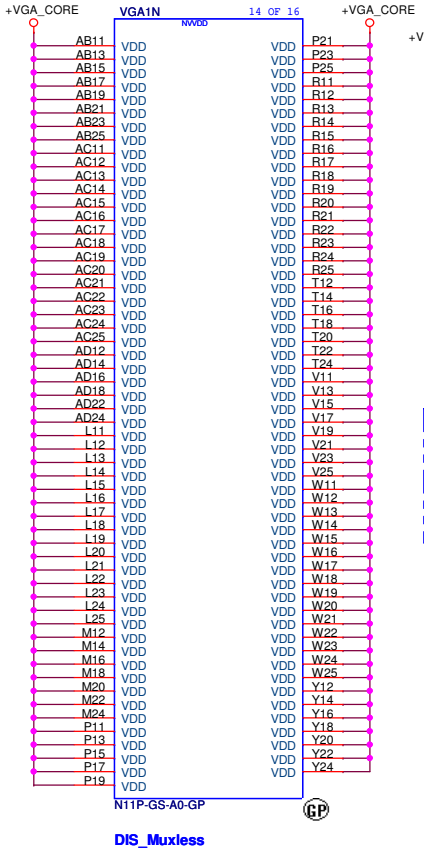

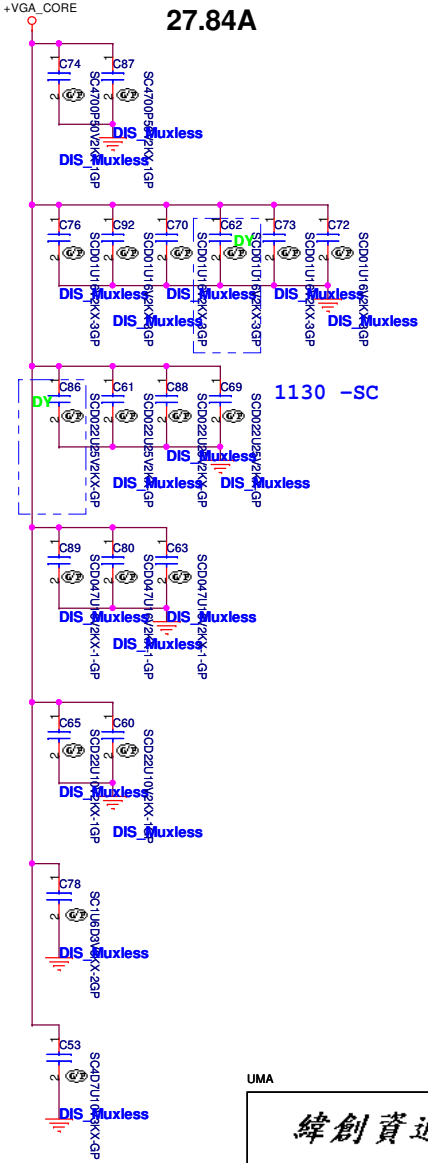

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Title: *N11P(6/6)_POWER*

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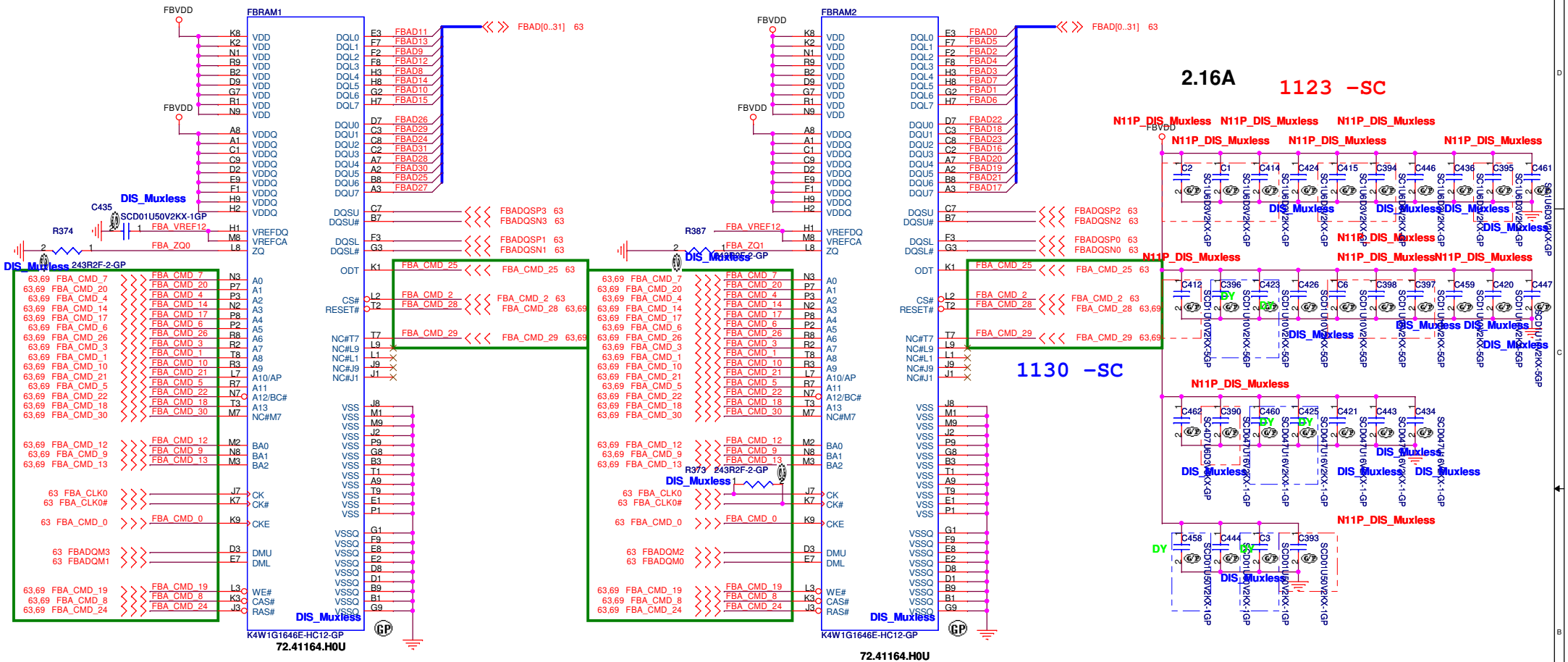
DDR3



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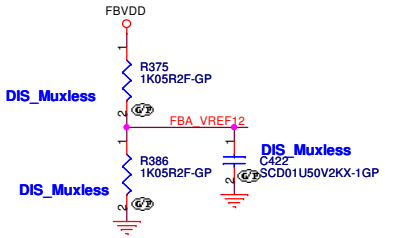
HYNIX: 72.51G63.C0U(Use OEM PN: VR.1GB0G.004)



UMA

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Title: *VRAM(1/4)*		
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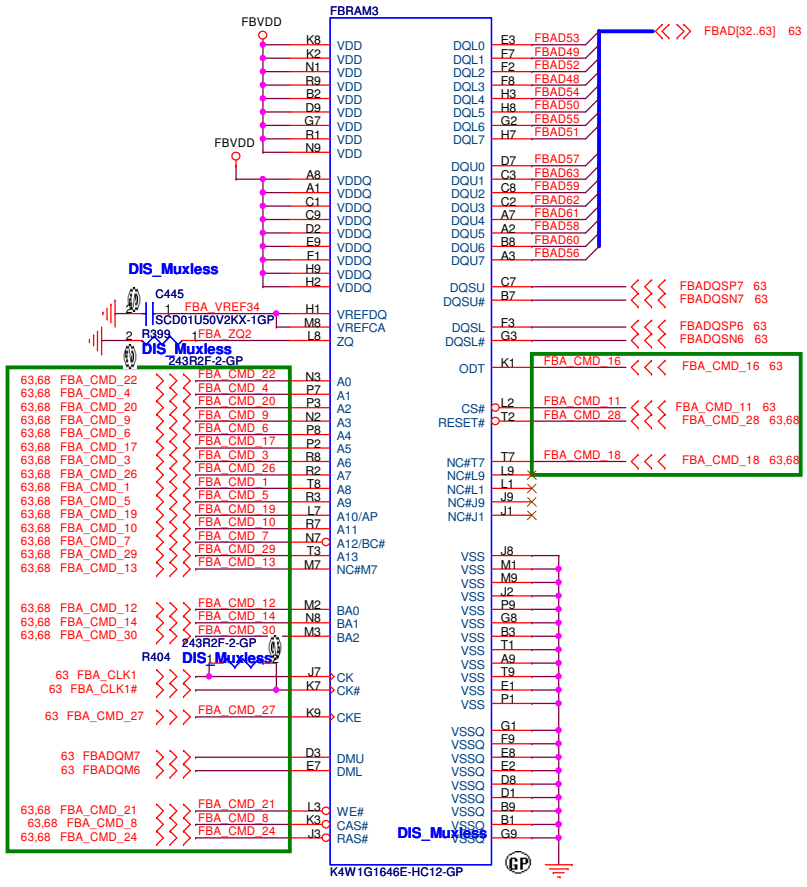
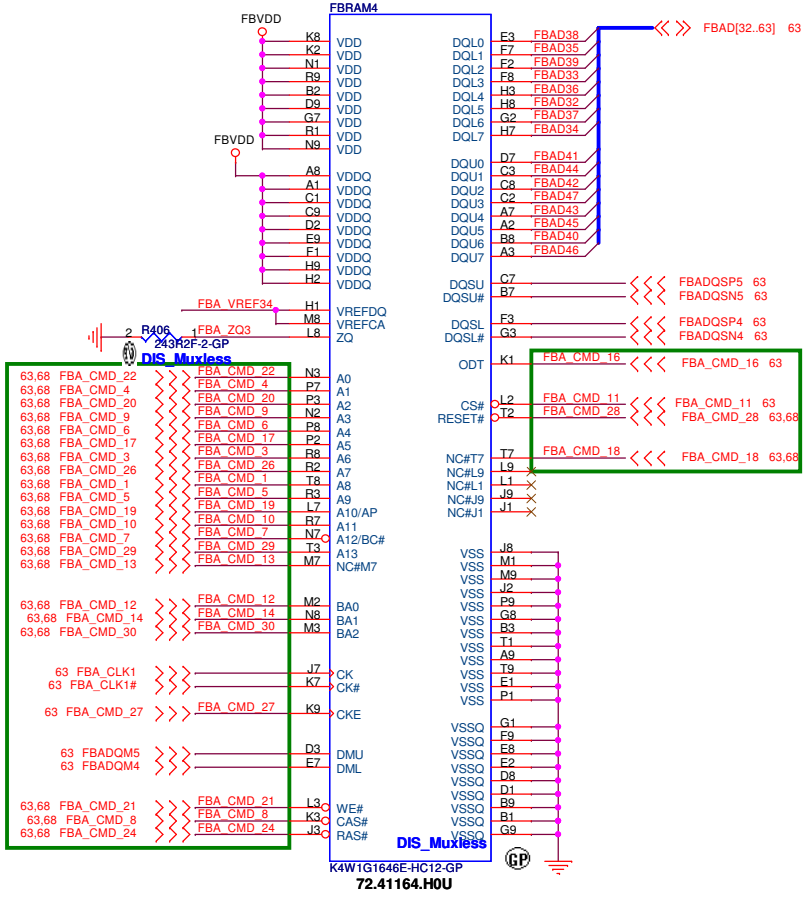
DDR3





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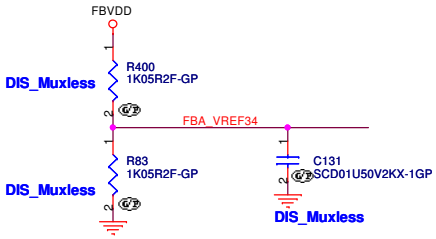
HYNIX: 72.51G63.C0U



HM42-CP

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Title	*VRAM(2/4)*	
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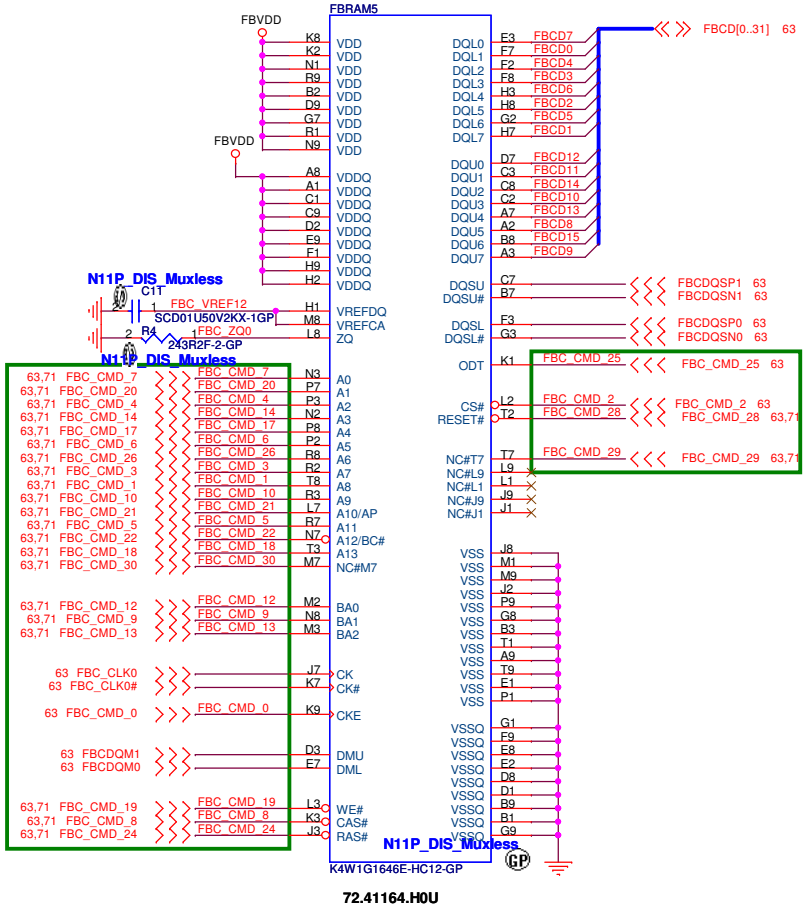
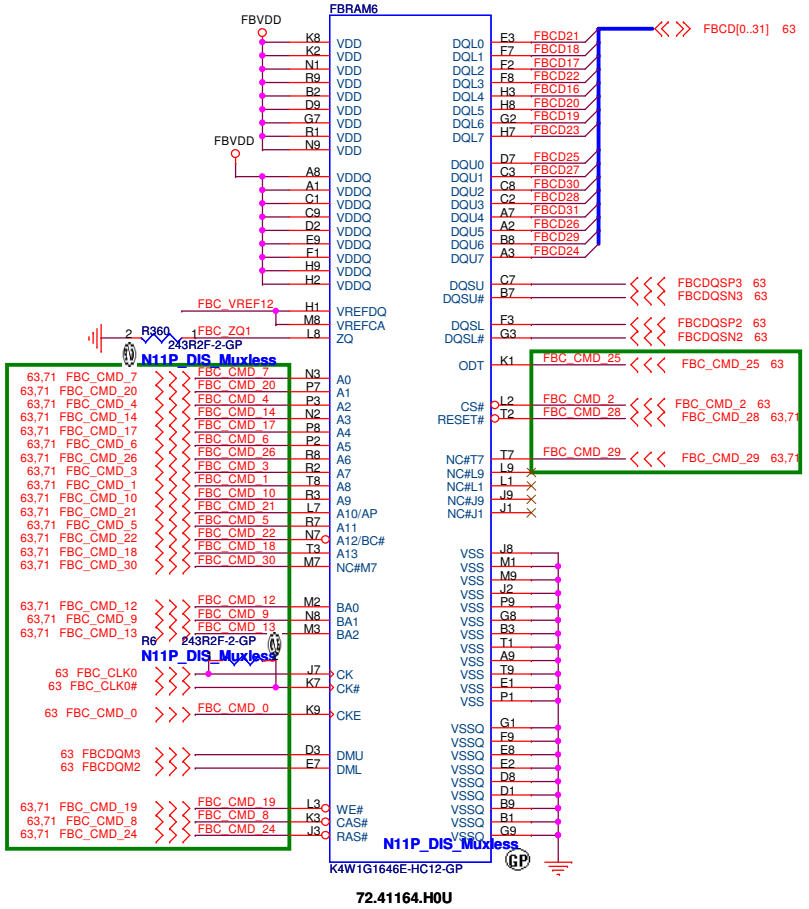
DDR3





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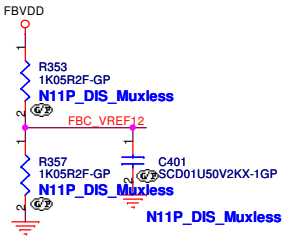

HM42-CP

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Title: *VRAM(3/4)*		
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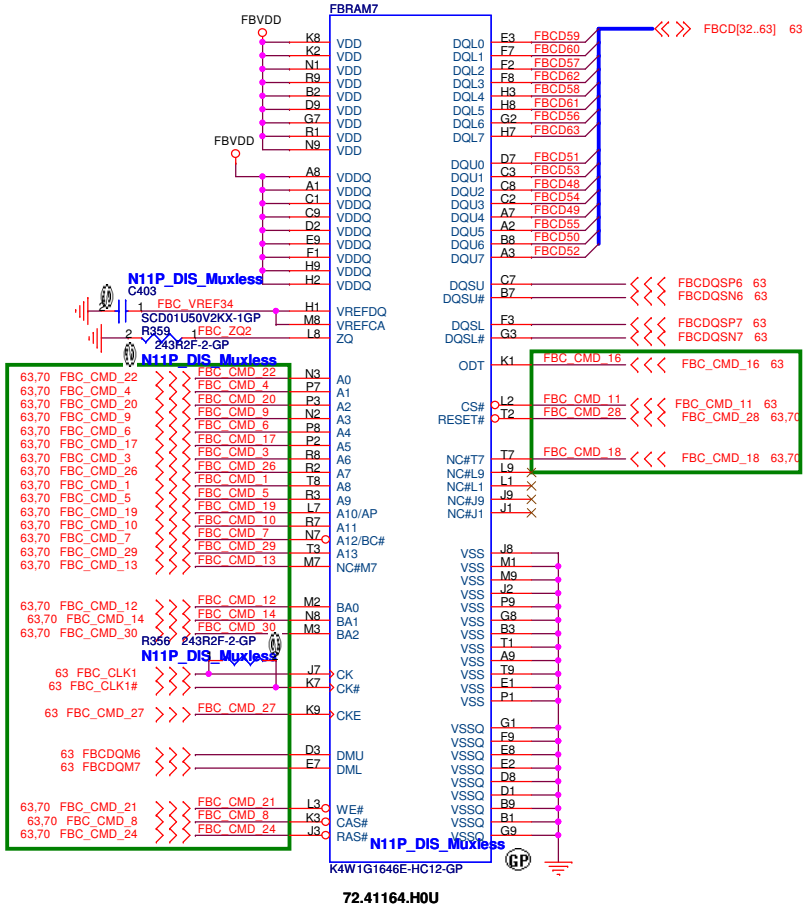
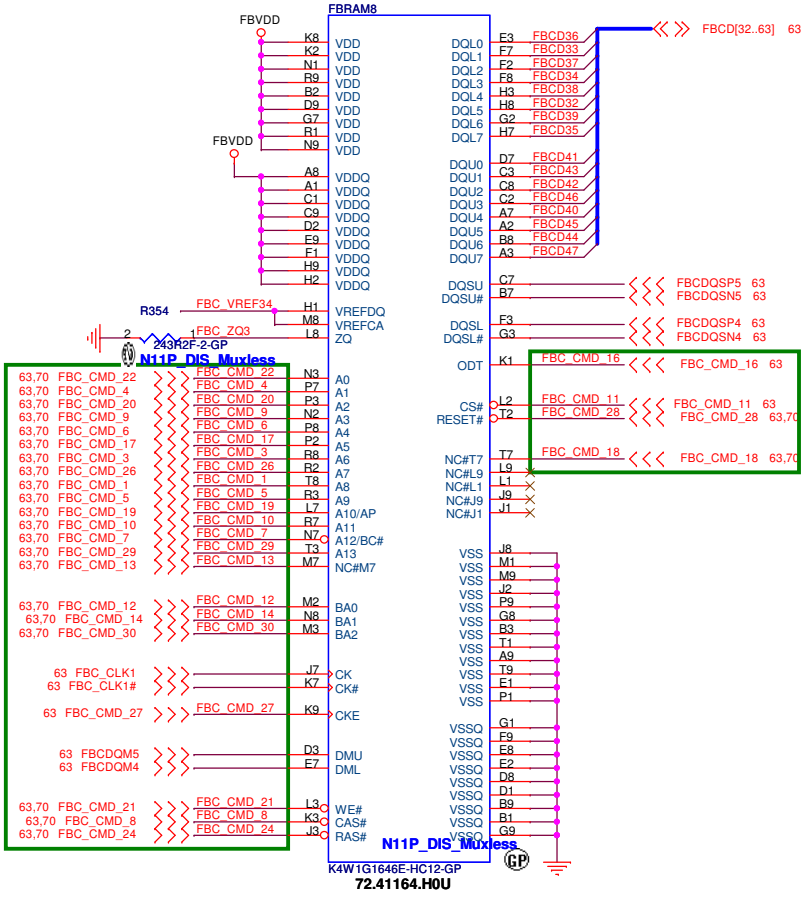
DDR3





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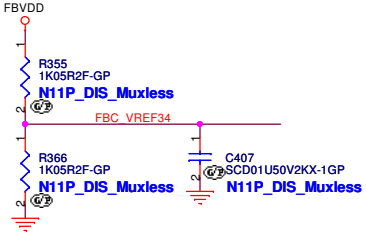
HYNIX: 72.51G63.C0U



UMA

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Title: ***VRAM(4/4)***

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3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006
Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confrim

[ECR]

Date	released by	ECR Number
11/22	Anita	R1001240

[Old]
PCH1 PN : 71.0IBEX.A0U
[New]
PCH1 PN : 71.0HM55.00U(KI.G5501.002)

[lab -SB]
2nd -> UMA (S01G)
1st -> Diserete N11P Hynix(S02G)
1st +3rd -> Diserete N11M Hynix(S03G)
2nd +4th -> Diserete N11M Samsung(S04G)
1st -> Diserete N11P Samsung (S05G)
2nd -> N11M Hynix_support Optimus (S06G)

[Eng -SC]
2nd -> UMA Non 3G (55.4GY01.S07G)
1st -> Diserete N11P Hynix_3G(55.4GZ01.S03G)
1st +3rd -> Diserete N11M Hynix_3G(55.4GY01.S09G)
2nd +4th -> Diserete N11M Samsung_Non 3G(55.4GZ01.S02G)
1st + 5th -> Diserete N11P Samsung _3G(55.4GY01.S10G)
1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]
UMA 3G (55.4GY01.M01G)
Diserete N11P Hynix_3G(55.4GY01.M02G) => 1st
Diserete N11P Hynix_Non 3G(55.4GY01.M03G) => 2nd
UMA Non 3G (55.4GY01.M04G)
Diserete N11M Hynix_3G(55.4GY01.M05G)
Diserete N11P Samsung _3G(55.4GY01.M06G) =>1 st
Diserete N11M Samsung_Non 3G(55.4GY01.M07G)

[PD action]
qual TPCN1 2nd source(20.K0296.006)
qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd
qual ODD1 3rd source(62.10065.E01)
qual PWRCN1 2nd and 3rd
qual RTC1 4th source
qual BT1 2nd and 3 source

qual U51 and U15 2nd source
qual TC13 2nd source(77.21571.111)
qual U32 2nd source
Qual HS1,HS2 2nd: 34.4B417.401

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Modify History
Size | Document Number: HM42-CP | Rev: SC
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